(NASA-CR-120619) DESIGN GUIDELINES FOR ADVANCED LSI MICROCIRCUIT PACKAGING USING THICK FILM MULTILAYER TECHNOLOGY (Electronic Communications, Inc.) 283 p HC $8.75 CSCL 09C G3/33

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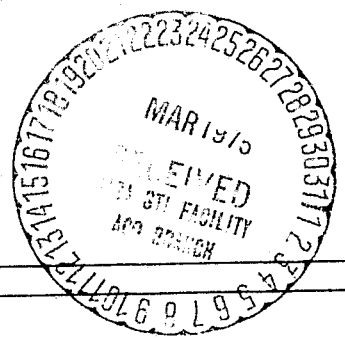
for

ADVANCED LSI MICROCIRCUIT PACKAGING

using

Thick Film Multilayer Technology



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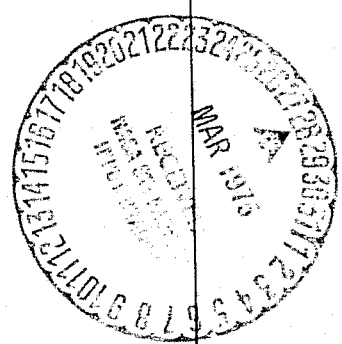
St. Petersburg, Florida



Marshall Space Flight Center
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

DESIGN GUIDELINES FOR ADVANCED LSI MICROCIRCUIT PACKAGING USING THICK FILM MULTILAYER TECHNOLOGY

By

C. J. Peckinpaugh

May 1974

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SECTION I

INTRODUCTION

1.1 Background

This document is the final report on Contract NAS8-29624, "Design Guidelines for Advanced LSI Microcircuit Packaging Using Thick Film Multilayer Technology."

These guidelines are intended as an educational tool compiled to inform designers and fabricators in the art of preparation and production of multilayer ceramic circuitry where the objective is to attain a high reliability end product.

Current state-of-the-art IC technology provides logic circuits which will change state in only one nanosecond. Operating speeds of computers have, therefore, reached a stage where speed can be limited by the length of an interconnection between integrated circuits. One method of reducing these lead lengths is by utilization of custom LSI chips. However, when special application monolithic LSI circuits are not available, significant lead length reduction can be realized by a hybrid approach. Ceramic multilayer interconnect systems permit the advantages gained through integrated circuit technology to be reliably utilized in a miniaturized custom-made form without incurring the expense and lead time involved in custom LSI chip design. However, as the physical size of the ceramic carrier interconnect circuitry decreases and active device density increases, the probability of electrical, thermal or mechanical problems increases proportionally. It is the objective of this design guide to alleviate wherever possible any post-fabrication problems by proposing a sound pre-production design philosophy.

1.2 Program Objectives and Approach

This report is a summary of the effort expended and conclusions reached during a 12 month study program. The overall program comprised three main phases of effort.

Phase I

This phase included a search for applicable technical papers and documents which could be used as reference material. Technical symposiums and seminars also were attended and referenced for applicable technical information. Where possible, authors of referenced literature were interviewed to determine additional technical details in relation to the published reference material. Particular emphasis was placed on the investigation and study of the following:

1. The maximum practical single substrate size based on mechanical stability of the most promising base materials, hermeticity provisions for active devices package processing environments, application environments, thermal dissipation requirements, accessibility for testing, ease of repair and optimum cost.
2. Computer aided design and artwork preparation.
3. Comparisons of the various processing methods such as screen printing, green-tape, plasma spraying, chemical vapor deposition, or other methods of fabricating hybrid LSI microcircuit packages using thick film multilayer technology.
4. Optimum interconnect construction analysis with consideration given the number of conductor layers, insulation layers line definition and component density.
5. The advantages and disadvantages associated with use of beam lead integrated circuit technology combined with screen printed thick film multilayer techniques.

Phase II

Based on the results of the Phase I study, test patterns were developed which demonstrated hybrid LSI microcircuit packaging technology and techniques. The description of these test patterns and design philosophy is found in the section pertaining to test pattern utilization.

Phase III

The final report is written to encompass the design standards and guidelines for present and future generation of ceramic multilayer hybrid microcircuit packaging. This report includes tables, graphs, diagrams, sketches, curves, procedures, photographs and drawings in sufficient detail to comprehensively explain the results achieved under this effort.

1.3 Organization of Report

This report is presented in four major sections as follows:

Section I - Introduction
Section II - Design guidelines with applicable process description, inspection information and procedures
Section III - Glossary of terms
Section IV - Technical references

1.4 International System of Units

For purposes of clarification, certain terms in this report have been presented in conventional terminology and units of measure. In compliance with the contract requirement concerning usage of international units of measure, (NBS Bulletin January 1971), the following list of conversions is presented in reference to NAS SP-7012:

To Convert From	To	Multiply By:
Inches	Meters	2.54×10^{-2}
Inches of mercury ($60^{o}F$)	Newton/Meter^2	3.37685×10^{3}
Inch^2	Meter^2	6.4516×10^{-4}
^{o}C	^{o}K	$^{t}K = {}^{t}C + 273.15$

SECTION 2
GUIDELINES

2.1 Abstract

Ceramic multilayer circuitry results from the sequential build-up of two or more layers of pre-determined conductive interconnections separated by dielectric layers and fired at an elevated temperature to form a solidly fused structure. The resultant ceramic interconnect matrix is used as a base to mount active and passive devices and provide the necessary electrical interconnection to accomplish the desired electrical circuit.

Many methods are known for developing multilevel conductor mechanisms such as multilayer printed circuits, welded wire matrices, flexible copper tape conductors, and thin and thick-film ceramic multilayers. Each method can be considered as a specialized field with each possessing its own particular set of benefits and problems.

This design guide will restrict itself to the art of design, fabrication and assembly of ceramic multilayer circuitry and the reliability of the end product.

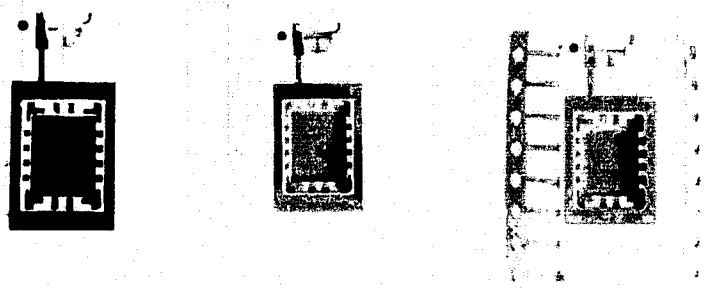
2.2 Ceramic Multilayer Interconnection

For the sake of simplicity, only the two primary methods of ceramic multilayer circuit design and fabrication will be discussed, "Green Tape" and "Screen and Fire" ceramic multilayer circuitry. As can be seen, the final end products of both methods are similar in physical characteristics but the method of obtaining each is significantly different.

2.2.1 Green Tape Method

The ceramic tape multilayer board (CTMB) was designed to provide a low cost (in large quantity), reliable, high density means of making crossover interconnections between devices to accomplish circuit functions. The technique employed is to fabricate a number of individual conductor layers printed on unfired flexible dielectric tape. The layers of conductors and dielectric are compressed and fired to achieve the desired multilayer circuit configuration.

Figure 2. 2-1 shows a ceramic package with buried conductors fabricated with the green tape method. Note the amount of material shrinkage which occurs during firing of the final structure.



Green Unfired Lamination | Fired Configuration | Package With Leads Attached Prior to Plating

FIGURE 2. 2-1

2. 2. 2 Screen and Fire Multilayer

As previously stated, the end product of the screen and fire ceramic multilayer fabrication is very similar to that produced by the green tape method. The main differences lie in the fabrication procedures.

The screen and fire fabricated multilayer substrate consists of sequential layers of conductors and/or resistors screen printed onto a ceramic substrate and separated with layers of screen printed dielectric. The layers may be individually furnace fired or co-fired depending on materials used. Windows are provided in each layer of dielectric to allow interconnection between conductive layers.

Figure 2. 2-2 shows a relatively simple screen and fired multilayer circuit utilizing integrated circuits on carriers. This circuit is part of an ultra high reliability electronic system.

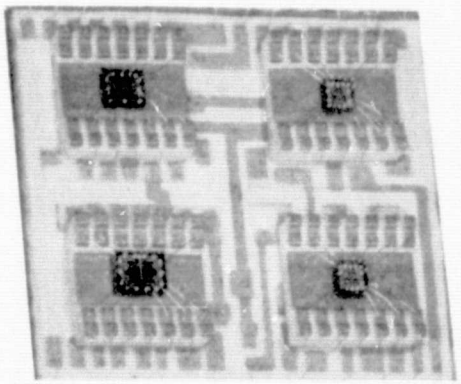


FIGURE 2. 2-2

Figure 2. 2-3 shows a complex 2 inch X 2 inch screen and fire ceramic multilayer circuit containing 44 beam lead devices prior to insertion into its carrier.

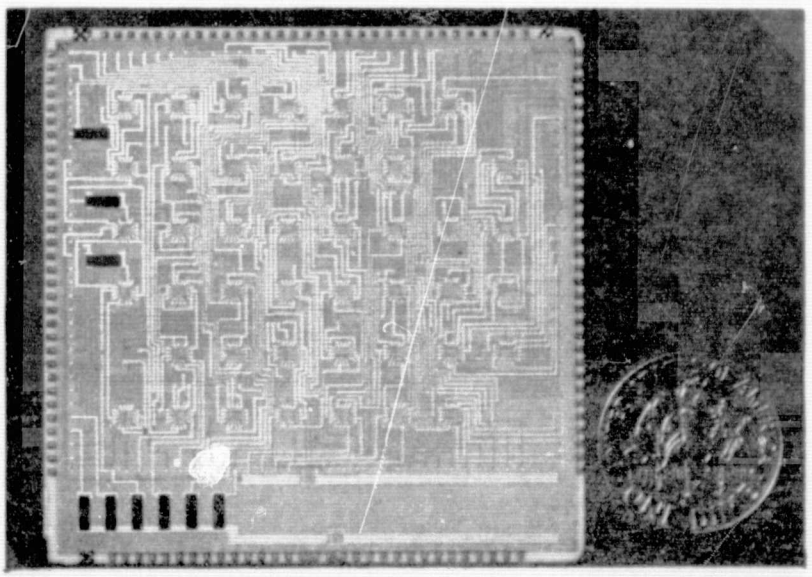


FIGURE 2. 2-3

2.2.2.1 Fired Cermet Conductor Layers Which are Etched Alternately With Screened and Fired Dielectric Layers

It has been demonstrated that etching the conductor pattern rather than screening the pattern itself can produce very good line resolution. This method of fabrication is the same as the one described in 2.2.2 except the conductor layers are screened and fired, then photoresist is spun, or sprayed over the entire substrate surface before etching the particular pattern. The dielectric with its properly located vias is then screen printed over the resultant conductor pattern. Generally, the conductor material is gold. Glassless conductor material can be spun or sprayed on the substrate, resulting in a uniform layer of conductor material, which is fired in a manner similar to typical thick film cermet paste. Photoresist is then applied to the continuous film of conductor material and the chosen pattern is exposed. Special etchants are used to remove the undesirable portions of the conductor layer. Technique type problems with photoresist and etching must be overcome to develop a process which yields fine lines consistently. Adhesion to the substrate or dielectric material has been shown to be another problem area.

2.2.2.2 Fritless Gold Conductor System

Glass-free gold thick film conductor paste (fritless) has recently been introduced to the microelectronic industry. The conductor pattern can be either screened or etched to produce fine line definition. The bond between the conductor material and substrate is a rather complex molecular one: therefore it may become necessary to develop dielectrics which closely resemble the alumina substrate to insure multilayer integrity. Line resolution is comparable to that of the better known cermet paste, but firing temperatures vary somewhat. The new fritless gold pastes are fired near 1000 degrees centigrade while typical cermet conductors fire in the 800 degree

centigrade range. The glass-free gold composition offers high electrical conductivity as well as high thermal conductivity. Beam lead bonding or thermocompression wire bonding should be quite good since the conductor material contains no glass. Soldering to the conductors will be prohibitive until newly formulated solderable glass-free materials are available from vendors. The cost of glass-free conductor pastes is relatively high compared to a typical thick film paste. It is conceivable that etching of these fritless materials might be easier and produce superior results when compared to standard cermet pastes.

2.2.2.3 Alternating Layers of Photo Printable Conductor and Dielectric Materials

Recently a new technology has been introduced which may prove to be worth investigating as a means of fabricating thick film multilayer interconnect systems. Utilizing particulate metals and inorganic oxides in a photosensitive vehicle, this material is either spun on like photoresist or sprayed on like paint. The thin coating of material is then selectively exposed to ultraviolet light through a mask and the unexposed material is washed away. The material is then air fired as are conventional cermet pastes to produce the desired pattern. At the present time, photoprintable gold conductor and low K dielectrics are available. The obtainable line resolution is 0.002 inches with 0.003 inch spaces. Since the conductor thickness is on the order of 0.0003 inches and a spray or spin application technique is used, the result may well be a film which more readily conforms to the undulating profile of typical thick film multilayer systems. These materials have the possibility of approaching the precision of thin film circuits.

2.3 Design Guidelines

The purpose of this section is to give the designer a set of standards to establish a working "envelope" in which to operate. Any design guide is only useful to the extent a designer employs it and the limitations and recommendations must be tempered with good judgment. For example, the establishment of a 0.005 inch minimum line width does not mean that a circuit should be designed using only 0.005 inch lines but the extremes should be used only where necessary.

It must be understood that the multilayer fabrication processes are critically dependent on both material characteristics (see Materials section 2.4) and workmanship standards of the operators performing the fabrication functions. These design standards will be more effective if employed in conjunction with an in-house materials evaluation.

A set of rules such as illustrated in this report can aid the designer in laying out planar arrays that will be practical for the process laboratory to fabricate within the limitations of present day equipment and technology. Prior experience in hybrid microcircuit technology is a prerequisite for a designer in order to effectively utilize these guidelines.

2.3.1 Electrical Circuit Design

The area of circuit design is of such a complex nature that only general recommendations can be made here. The basic circuit design should be closely checked for applicability to multilayer package design. As in the case with substrate layout, the electrical designer should have a working knowledge of fabrication and substrate packaging procedures.

The basic circuit design considered for multilayer application may be a conventional circuit or an entirely new design.

In either situation, a schematic and a diagram will be prepared showing the elements that are to be produced along with the external connections. There are a number of restraints, such as size limitations, compatibility with the next level of interconnections, etc., that must be kept in mind.

2.3.1.1 The Breadboard

Using the original circuit diagram, the next step is to produce a sample circuit or breadboard to see how it operates. Alterations of the original circuit design can be made based on the operating characteristics of the breadboard circuit saving expensive redesign if made later in the process.

Breadboards in discrete component form usually offer accurate indications of final hybrid circuit performance, but circuit operating characteristics are sometimes affected by the hybrid film circuit. This occurs because of differences in operating characteristics of the various component forms.

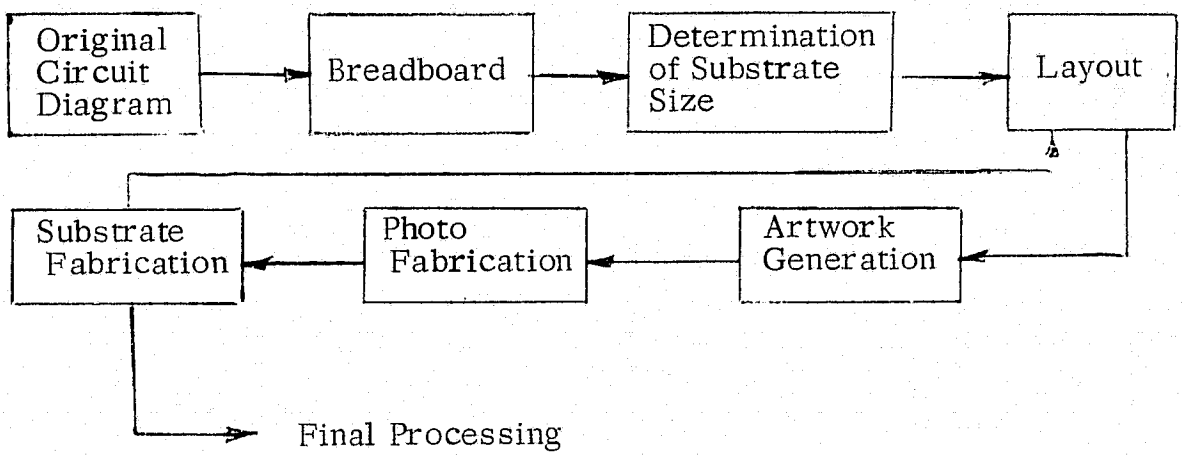
Thick film resistors will have different noise levels and different TCR's than discrete resistors usually used for the breadboard. Thick film capacitors may also differ from the breadboard capacitors. To some extent, this can be compensated for by using thick film discrete components (with leads) whose operating characteristics will be much more similar.

Active devices mounted on the substrate and connected by gold or aluminum wire may perform quite differently than the same chips mounted in a discrete package with leads as used in the breadboard.

The difference in size of the breadboard and the final thick film circuit can result in different operating characteristics. Smaller size and shorter conductor runs make for shorter propagation times and lower inductance in a thick film multilayer circuit but also promote greater inter-element capacitance. Capacitance difference can be minimized by adding phantom components to the breadboard that will imitate the expected parasitic capacitance. It is difficult to compensate if the breadboard is adding inductance to a lead. The final thick film circuit will often operate with improved characteristics. If the breadboard can be made to operate satisfactorily, then the final hybrid design has a good probability of exceeding this performance.

The breadboard approach will work for many applications but is inappropriate for other applications. Breadboard performance for high frequency and other critical circuits often does not correlate well and the breadboarding step is eliminated by going to actual thick film prototypes instead. If this is the case, much emperical engineering is done by going through two or three separate thick film layouts.

2.3.1.2 The Design Sequence



2.3.2 General Design Considerations

Prior to actual layout of physical dimensions for the multilayer substrate, the following general design rules must be considered.

2.3.2.1 Maintain circuit identity and function if possible. The same packaged electronic function (such as a saw tooth generator) may be used in other applications. Trouble-shooting is also aided considerably by having a distinct circuit identity.

2.3.2.2 Choose appropriate discrete component types and the method of assembly. Obviously, the advantages gained by miniaturizing an electronic circuit would be lost if the package were required to house large bulky components that do not lend themselves to miniaturization.

2.3.2.3 Make maximum use of standard IC's and LSI arrays. Check availability of all parts. The cost factor may become significant when using non-standard parts. Availability may become a serious burden on delivery schedules.

2.3.2.4 Holes in ceramic substrates should be avoided if possible. Holes must be formed in the green tape state unless ultrasonic or air abrasive drilling is used. Reliable connections are difficult to make through holes in ceramic substrates.

2.3.2.5 Use only one side of a substrate since screen printing and firing on both sides of a substrate complicates processing and can adversely affect yield and fabrication time.

2.3.2.6 Use preferred dimensions. Minimums should be used only where preferred dimensions are not practical.

2.3.2.7 Conductor runs should be kept as short as possible to minimize resistance and lessen opportunity for physical defects.

2.3.2.8 Avoid running conductors around edge of substrate if possible. Edge printing requires special tooling and substrate preparation. Yield and reliability as well as fabrication times may be adversely affected.

2.3.2.9 Orient resistors in either the "X" or "Y direction for ease of trimming.

2.3.2.10 Printed resistors should be located on the bare substrate and not allowed to contact the dielectric material. (see Test Pattern Utilization section.)

2.3.2.11 Prepare a parts list which includes (a) dimensions (b) contact pads or leads and materials (c) number of connections required (d) possible substitutions (e) power requirements and (f) unique limitations.

2. 3. 2. 12 Determine substrate size based on optimum packaging conditions (see Determination of Substrate Size, 2. 5. 3).

2. 3. 2. 13 Jumper wire crossovers may be used when one or two per substrate will eliminate one or more screening operations.

2. 3. 2. 14 Coordinates should be parallel to the "X" or "Y" axis and established from the lower left corner of the circuit. All film elements and discrete components should be laid out parallel to the "X" or "Y" axis with exceptions being made for beam lead conductor lines.

2. 3. 2. 15 The scale used for layout is not critical; however, the layout can be facilitated by considering final conductor line sizes when choosing the scale. For example, a 25:1 scale is convenient for .008 inch line width while a 20;1 scale is more convenient for .010 inch line width. Mylar or vellum grid paper with 10 divisions per inch will facilitate layout.

2. 3. 2. 16 Avoid closed loops A circuit design may call for a closed conductor/resistor loop. To make possible measuring and trimming of resistors, this loop must be broken until assembly of the circuit is begun. It may then be closed with a wire jumper.

2. 3. 2. 17 B+ and ground lines should be maintained on the same conductor level whenever possible. Use interdigitated patterns to better utilize feed-ins to components.

2. 3. 3 Determination of Substrate Size

Before an actual layout can be started, a physical size limitation must be established. Many factors contribute to the determination of the most efficient size and configuration of the base substrate. Some of the most significant are end item cost, mechanical and electrical parameters, power requirements and system packaging philosophy.

2.3.3.1 End Item Cost

Very few, if any programs exist today where end item cost is not an important factor. Receipt of contract or delivery of hardware may very well depend on a narrow margin of cost versus selling price markup. The determination of "to buy or build is primarily an economical exercise as technology or processing equipment are purchasable items. Determination of repairability versus throw away is usually set at an end item cost of $500.00. Less than $500.00 unit cost usually categorizes a circuit as a throw away item. Determination of maximum allowable cost per package must be accomplished before circuit function partitioning may be accomplished.

2.3.3.2 System Partitioning

Initially, the overall system design is partitioned into functional subsystems. The size and complexity of those subsystems usually determines the size of the substrate. The multilayer circuit is then designed for an optimum between reliability and high density packaging. In digital circuits, the required device area per gate has been empeirically derived to be

$$A/n = C^2 (n^{1/3} + 4n^{-1/3})$$

Where

A = area
n = number of gates
C = bonding pad width and spacing

Plotting this equation versus the number of gates in Figure 2.3-4 shows that the area/gate is somewhat constant up to 100 gates, then the A/n rapidly increases with the number of gates. This indicates that integration beyond a certain level will decrease the package density of the system.

The number of unique parts that should be utilized in a digital design is determined by the use of either integrated circuits, MSI devices or LSI devices. The curve in Figure 2.3-5 points out that the parts count can be decreased by incorporating LSI chips. The most efficient and economical design

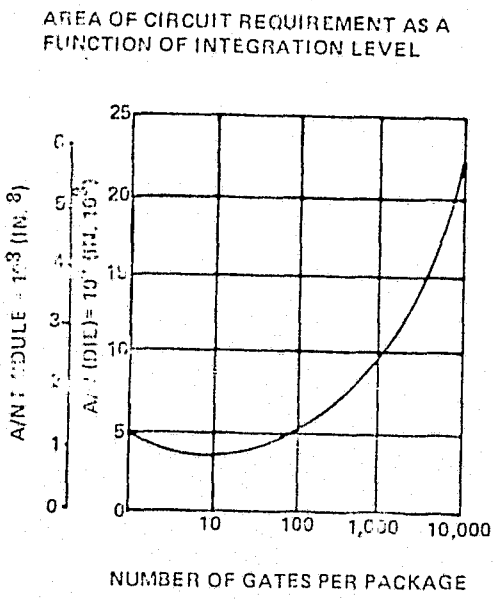


FIGURE 2.3-4 . AREA/GATE VERSUS GATE COUNT

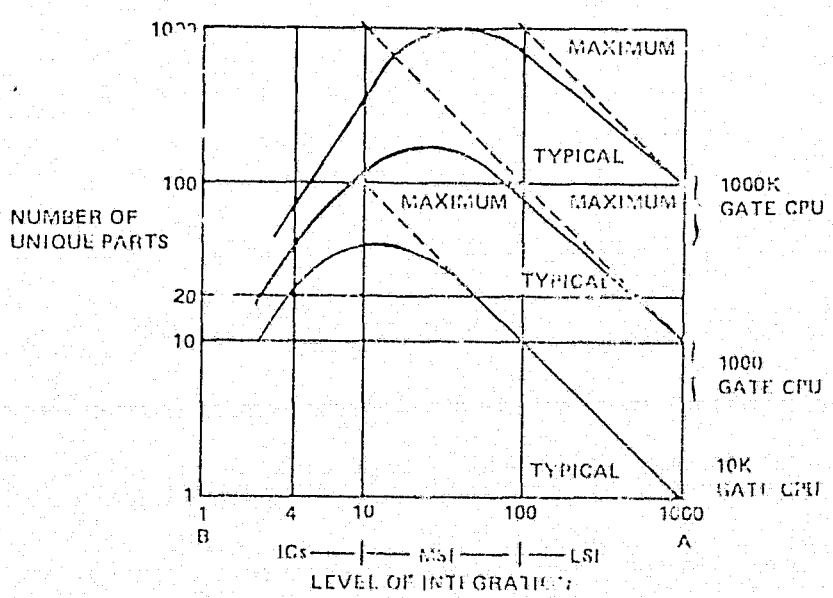


FIGURE 2.3-5. NUMBER OF UNIQUE PARTS VERSUS INTEGRATION LEVEL

for a hybrid multilayer circuit is generally obtained by using some combination of the three chip types. Furthermore this design approach will save design time and expense when existing devices are utilized.

Then, too, there are other considerations such as substrate material availability, package availability, and/or cost if developing and fabricating special materials and packages. If too large a multilayer interconnect board is designed, problems resulting from processing tolerances, registration from layer to layer and mechanical and physical stresses can become unmanageable.

2.3.3.3 Power Limitations

Total circuit power dissipation should be limited to 1.5 watts/inch^2. This is only a rule of thumb and must be determined by the overall thermal design, the maximum junction temperature and the maximum system temperature. The thermal resistance of any given device can be calculated with the equation:

$$\Theta = \frac{t}{KA}$$

Where:

t = thickness in direction of heat flow
K = thermal conductivity of medium
A = cross-section area

In actual practice, it may be difficult to achieve the calculated thermal resistance. For example, a eutectic bonded device may have a void in the bond interface which would increase the thermal resistance. Initial calculations indicate that direct die attached devices have 20 to 50% lower thermal resistances than beam lead devices. Due to the reproducibility of beam lead devices and the common occurrence of voids in directly attached devices, both methods are specified to have nearly the same thermal resistivity. Conformal coatings decrease the thermal resistance for either method of device attachment but the effect is much more pronounced in beam lead devices, especially

as the power is increased. Of course, power generated internally in relation to the ambient temperature will determine the amount of heat removable from a package. The total power dissipation is a summation of all power generating components per total substrate area.

2. 3. 3. 4 Substrate Availability

The 96% alumina substrate is available in a rather large assortment of sizes and shapes. The most readily available standard size appears to be the 2 inch X 2 inch and 1 inch X 1 inch in both . 015 inch and . 025 inch thicknesses. These basic sizes may be further reduced or altered by sizing before or after processing. Surface conditions also play an active role in determination of substrate size as the normal processing camber is usually specified at . 004 inches/in of substrate. In large substrates, this camber would reduce the screen "break-away" which is normally . 025 inch by a significant amount. A 3 inch X 3 inch substrate could conceivably have the screen "break-away" reduced by almost 50% thereby critically affecting definition.

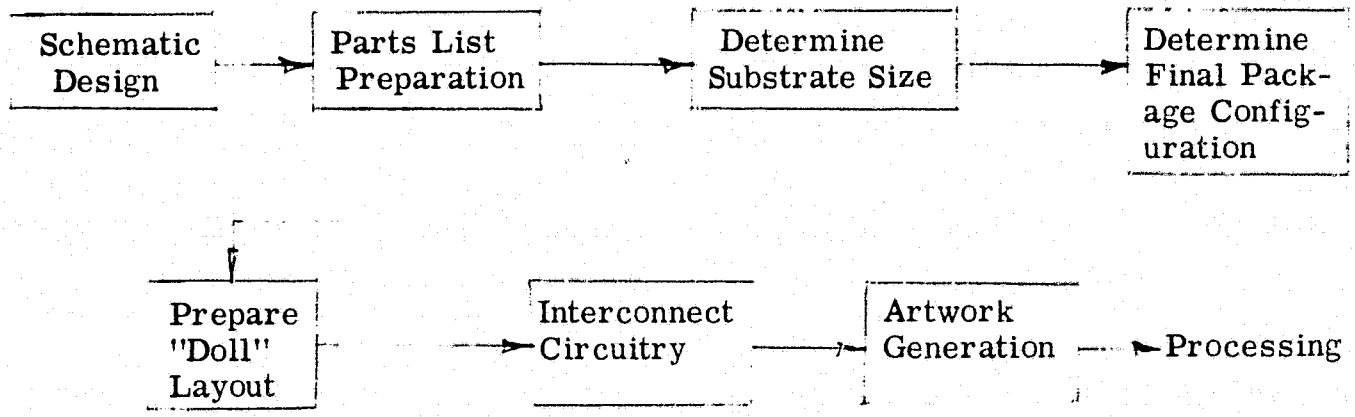
2. 3. 3. 5 Packaging Method

Substrate size may become a critical factor when considering hermetic sealing of end item circuitry. Flatpacks or carrier packages are limited in availability. Sealer configruation may be a determining factor also.

2. 3. 4 Layout Procedure

The following discussion concerns the procedures and techniques used in transposing a given circuit electrical schematic into a working" layout from which the actual fabrication artwork can be produced.

As stated, it is extremely important for the substrate designer to be familiar with the manufacturing processes as well as the electrical and mechanical characteristics which affect the final deliverable circuit. The following sequence of events should be followed after gathering as much information concerning the circuit as possible:



2.3.4.1 Schematic Diagram

As indicated previously, circuit functions may be altered or revised due to interreactions and adverse circuit characteristics which show up during the breadboard stage of circuit design. The engineering schematic can be drawn after all problems have been worked out of an electrical system and a final circuit function or segment identity has been decided upon.

The schematic should clearly show component identification values and tolerances. Interconnections between components should be shown with any sensitive areas labeled for special consideration during layout.

2.3.4.2 Parts List Preparation

An engineering parts list should be prepared which shows the following information at a minimum:

1. Part (resistor, capacitor, etc.)
2. Reference Designation (R1, C1, etc.)
3. Value
4. Tolerance (± 5% etc.)
5. Vendor (from whom purchased)

6. Vendor Part Number
7. In-house Part Number
8. Component Size (dimensions and break-outs)

Figure 2.3-6 shows a typical engineering parts list used in the layout phase of development. See Selection of Discrete Components and Substrate Element Design sections (2.3.5 and 2.3.6).

2.3.4.3 Determination of Substrate Size

This subject has been covered previously but should require special study as the substrate size can be a very influential factor in circuit performance.

2.3.4.4 Determine Final Package Configuration

This function should be considered one of the most important steps in the layout procedure as the final packaged circuit must be capable of surviving in the hostile environments encountered after leaving the special handling that it will enjoy during fabrication and assembly. See Selection of Discrete Components section for information on package selections (2.3.5).

2.3.4.5 Prepare "Doll" Layout

The approximate component area consumption and orientation can be determined by the use of component representation "dolls".

The representative dolls are drawn to scale using the scale of the layout as a basis. Each component doll should be drawn to the maximum tolerance dimensions using vendor information or in-house data files. The dolls should also include any connecting pads with the component terminations shown. The termination areas or connecting pad area sizes may be determined by bonding and electrical connection method. Figure 2.3-7 shows typical component dolls for use in the layout phase.

Screened on components such as resistors, capacitors and inductors should be calculated as covered in their respective subsections under Substrate Element Design (2.5.6).

CIRCUIT NO. _____ CIRCUIT TITLE _____ THICK FILM ____ THIN FILM ____

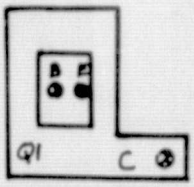
ENGINEER _____ DATE _____ DEPT _____ REV ____ DATE _____ REV ____ DATE _____

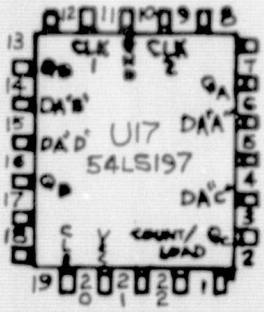
DESIGNER _____ DATE _____ CKT. NO. _____ REV ____ DATE _____ REV ____ DATE _____

PART	REF. DES.	VALUE OR TYPE	TOL	QTY	VENDOR	VENDOR NO.	COMPANY NO.	CASE SIZE	REMARKS

NOTES:

Typical Engineering Parts List
FIGURE 2.3-6





Capacitor Chip

Transistor Chip with Die Braze Area

Beam Lead IC Device

FIGURE 2.3-7

2.3.4.6 Interconnect Circuitry

2.3.4.6.1 Paper Layout

For the first trial layout, place the dolls of the specific components to the approximate positions of the schematic diagram and then shift them around for better physical fit. This procedure will generally reveal potential interferences.

Redraw the screened components and sketch in the conductors and leads and the estimated outline of the substrate to scale around the cutouts. The trial layout can be used to check the required substrate size, to provide a visual description of the component sizes and dsitribution, and to show major interferences, such as blocked-in terminals requiring crossovers, and other topological difficulties.

This trial layout, if satisfactory, becomes the model from which all elements are detailed carefully, tailored to fit oddly shaped spaces, and recalculated to ensure that they meet design values. The interconnect conductors and isolation crossovers are also placed with the dimensions selected from the applicable sections (see Substrate Element Design section 2.3.6). Naturally, components will have to be moved as conductors are accurately drawn in, and any further difficulties may have to be resolved by cut-and-try: i.e., by starting a different translation of the schematic and a different trial layout. (some engineers even

use a Polaroid camera or a Xerox machine to record each trial layout before changing or revising it.)

2.3.4.6.2 Breadboarding by Layout Simulation

An extremely useful way of checking the circuit layout for correct operation and such effects as ground loops or undesirable proximity of parts is to construct a simulated layout with breadboard components. Miniature packaged parts of sizes approximating the components to be used can be wired together by hand; perhaps too laborious for a very complex circuit, but very useful in many other cases. Some hybrid laboratories use blank substrates to which the main parts can be assembled to simulate the layout of the more critical components.

As experience is gained, the engineer will find that making screens for a revised circuit is not too expensive and should not deter him from experimentation. The first actual hybrid prototype will serve as a simulated breadboard, and changes may very well result from the measured performance parameters. A breadboard can usually be tested and evaluated in essentially the same manner as a prototype design prior to actual artwork commitment.

2.3.4.6.3 Layout Revisions

Some of the changes which might be considered in subsequent revisions and iterations of the design are:

1. Substitution of chip components for printed components occupying too large an area or not meeting electrical requirements.
2. Substitution of printed components for chip components if sufficient area is available and appropriate characteristics match.
3. Change of basic material resistivity for resistors or dielectric medium for capacitors.
4. Change in the number of screening operations.
5. Use of a finer or coarser basic line width.
6. Use of a different range of semiconductor devices and mounting methods, such as chip and wire, beam lead, or packaged microdevices, to achieve better size, yield or cost.

7. Rearrangement of layout of circuit and lead wires to minimize crossovers, separate appropriate circuit segments from each other and minimize common critical ground currents.
8. Revision of resistor size or component locations to keep power dissipation within reasonable limits; this may also involve changes of substrate size.

From several successive approaches to the layout of each circuit, the designer will often develop additional trade off rules as he gains confidence and thus speed up the initial design choices.

2.3.5 Selection of Discrete Components

At the present time, the list of vendors who supply discrete components for hybrid microcircuits is quite large. For some time, the component manufacturers were reluctant to commit their fabrication facilities to the volume required to bring the price of discrete components down to the "users" level. With the advent of large scale acceptance and use of hybrid microelectronics, the trend is now to greater availability and lower cost of discrete parts.

The components most applicable to multilayer hybrids can be grouped as follows:

1. Chip Capacitors
2. Chip Active Devices
3. Mini-components
4. Special Termination Devices
5. Packages
6. Chip Resistors

2.3.5.1 Chip Capacitors

It has been found that chip capacitors are the most economical in both space consumption and processing costs when compared to deposited substrate element capacitors.

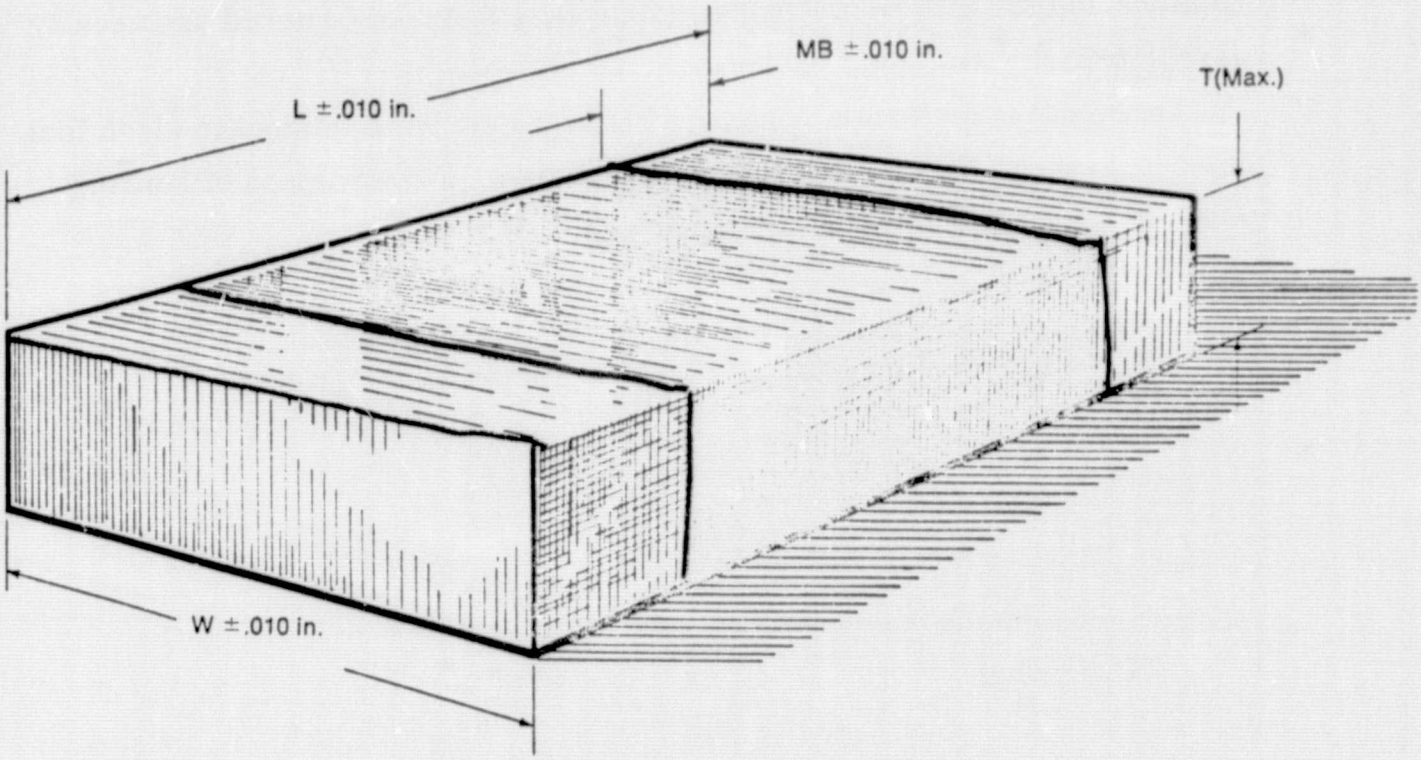
The add-on chip capacitors are available in single dielectric layer and multilayer form. The multilayer type chip is slightly more expensive but more widely accepted due to the extremely wide capacitance range and terminating methods available.

A number of formulations are available, but two basic types used most frequently are high "K" and low "K" (NPO types). Both types of chip capacitors are available in a wide range of values and sizes and tolerances ranging from ± 1/2 to ± 20%. Reliability has been proven to be extremely high in chip capacitors and the failure mechanisms that have been encountered are usually associated with assembly operations.

Termination materials become a critical item when related to electrical interconnect method. The following chart shows a comparison of bonding methods to various termination materials.

Electrical Contact Method	Termination Material
Solder	Silver Pd/Au Pt/Au Platinum Pd/Ag
TC Bonding	Gold Pt/Au Platinum
Conductive Epoxy	Silver Pd/Au Pt/Au Platinum Gold

A good quality control and inspection program is recommended to assure integrity of the components.



Summary of Characteristics of Materials Currently Available

Type	Dielectric Constant	Temperature Coefficient	Operating Temperature Range	Dissipation Factor	Typical Cap Δ With DC Voltage Bias	Typical Cap Δ With AC Voltage Bias
COG/NPO	80	0 ±30ppm/°C	−55°C to +150°C	.05%	0%	0%
COG/NPO	80	0 ±10ppm/°C	−55°C to +150°C	.05%	0%	0%
W5R/BX	1600	±15% Max	−55°C to +125°C	2.0%	−10%	+20%
K2000	2000	±15% Max	−55°C to +125°C	2.0%	−20%	+20%
K2500	2500	±15% Max	−55°C to +125°C	2.5%	−25%	+20%
K5000	5000	+20% −50%	+10°C to + 85°C	2.5%	−40%	+30%
K5000	5000	+20% −85%	−55°C to +125°C	2.5%	−40%	+30%

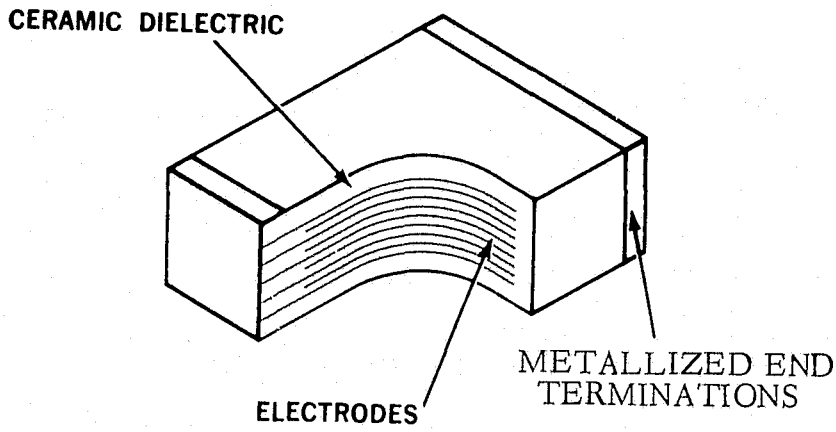


FIGURE 2.3-8 TYPICAL CHIP CAPACITOR

2.3.5.2 Chip Active Devices

Most integrated circuits, transistors and diodes which are available in packaged form are available in chip form. When designing a multilayer circuit using chip devices, consideration should be given to specialized assembly and termination methods such as die brazing and TC bonding. Reliability can also be adversely affected if absolute process control is not maintained.

2.3.5.3 Mini Components

Mini components are those circuit devices which are cased in some type of package or protective covering with leads available for electrical termination. These devices have a tendency to use a large amount of space due to their larger bodies and the terminating pad areas required for the package leads.

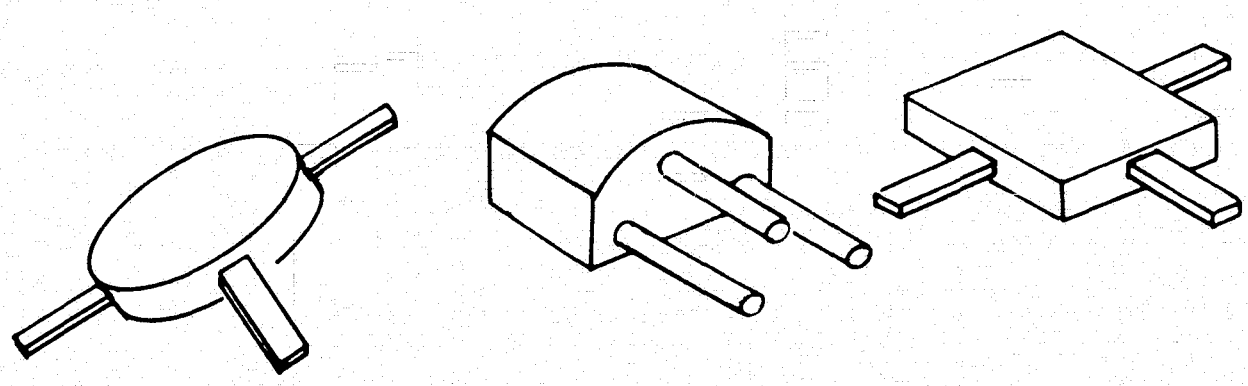


FIGURE 2.3-9 TYPICAL MINI COMPONENTS

2.3.5.4 Special Termination Devices

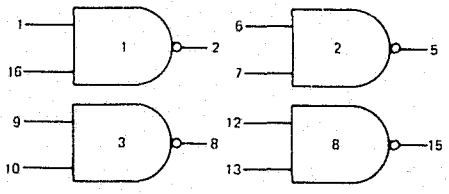
This class of components includes the beam lead devices, "flip chip" and lids (leadless inverted devices). The most desirable type of device for high density multilayer use is the beam lead device. The devices themselves are considered hermetically sealed and some are able to withstand handling that would be destructive to planar process chip devices. Most active devices that are presently available in chip form are also available as beam leads.

TYPICAL AVERAGE PROPAGATION DELAY TIME = 16nsec

TYPICAL TOTAL POWER DISSIPATION = 8mW

SSI LOGIC EQUATION

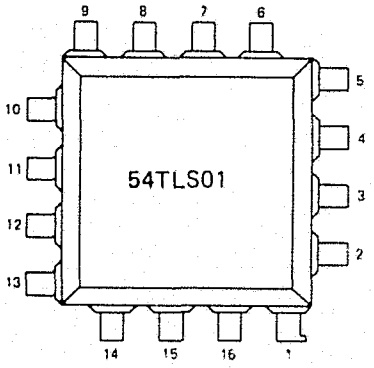
POSITIVE LOGIC: $Y = \overline{AB}$



BEAM-OUTS

1. 1A	9. 3A
2. 1Y	10. 3B
3. V_{CC}	11. GND
4. NC	12. 4A
5. 2Y	13. 4B
6. 2A	14. NC
7. 2B	15. 4Y
8. 3Y	16. 1B

EIA STANDARD CHIP DIAGRAM



(Top View)

FIGURE 2.3-10 TYPICAL BEAM LEAD DEVICE

Flip chips are not quite as available or popular as beam lead devices. The main reason for the lack of popularity is the difficulty of bonding and the difficulty of inspection of the electrically bonded unit.

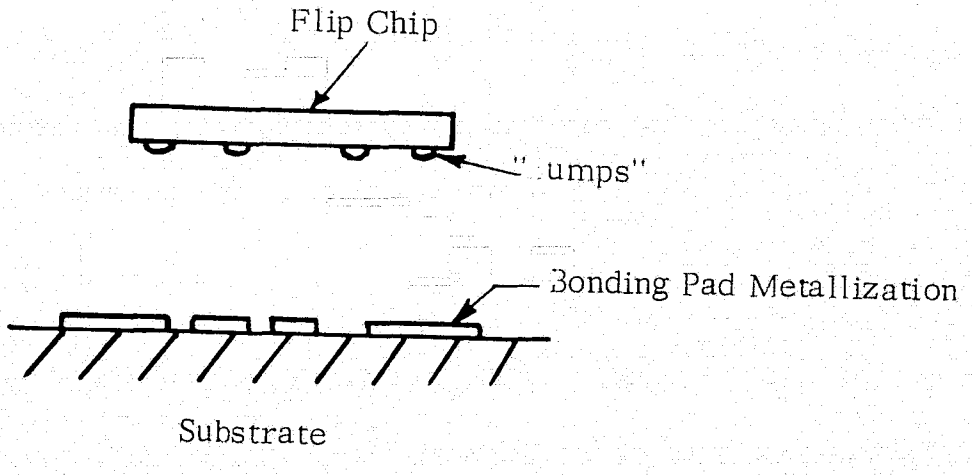


FIGURE 2.3-11 FLIP CHIP MOUNTING METHOD

The "lid" devices are discrete chip devices which have been mounted on and electrically connected to a carrier device. External electrical connections are made to pads provided on the carrier. Space consumption is more significant when compared to the other forms of devices but ease of handling and ability to burn in devices and perform extensive pre-assembly testing makes use of lids inviting. "Lid" devices may or may not have encapsulation depending on the application and device type.

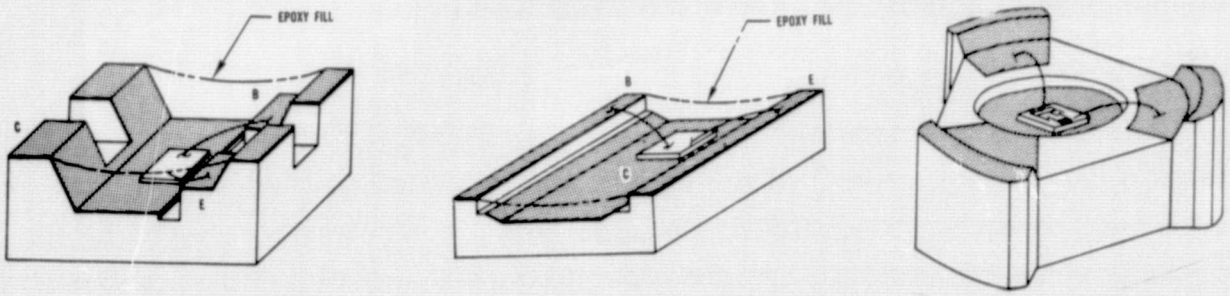


FIGURE 2.3-12 LID (LEADLESS INVERTED DEVICE)

2.3.5.5 Packages

Although packages have no direct role in a thick film circuit (electrically) they nevertheless represent a most important part of the overall technology of building thick film circuits. It is unfortunate that because of their secondary electronic role, the technology of packaging is at times given insufficient attention. The package is an extremely important and critical consideration often responsible for making or breaking a thick film design (from a performance and/or an economic standpoint).

2.3.5.5.1 Package Functions

There are three functions of packages in thick film circuits

1. They protect the circuit from the physical environment in which the circuit is to be operated and provide a benign ambient for sensitive components.

2. They may be required to protect the circuit from EMI, EMP or related interference with circuit operation.
3. They provide for electrical and thermal paths between the circuit and its surroundings.

2.3.5.5.1.1 Protecting the Circuit from the Outside Environment

Thick film components themselves generally are fairly rugged but where unencapsulated silicon chips or other discrete components are present, a protective system of some kind is usually necessary. Some of the types of environmental situations that arise are described below.

2.3.5.5.1.1.1 Humidity

It is of utmost importance that a thick film circuit receive adequate protection from water vapor. If the circuit was intended to operate in a protected area such as an air conditioned room, the humidity protection offered by the package could be minimal. At the other extreme, most circuit specifications require operation in high humidity environments. This range of humidity levels makes for a variety of packages. Furnishing adequate humidity protection is perhaps the most demanding task for packages.

2.3.5.5.1.1.2 Contamination

Thick film multilayer hybrid circuits often operate in situations where protection from chemically active materials is needed. In many situations, a simple contamination may end up as a corrosive substance. Residues such as flux and epoxy hardners can, under certain conditions, combine with moisture to form electrolytes which support catastrophic electrolytic corrosion.

2.3.5.5.1.1.3 Abrasion, Pressure, Shock and Vibration

These situations quite obviously generate need for protection of the thick film circuit. The flying leads of a silicon chip cannot tolerate handling of any kind. A package with this kind of lead bonding must be designed so that nothing can disturb the circuit. Total physical isolation is essential. Other components, while firmly attached for normal use, may need protection if the environment or the application of the circuit involves acceleration such as is encountered in missile use, pressure at great depths in an ocean,

vibration from a vehicle or being dropped (shock).

2.3.5.5.1.1.4 Electrical Protection

Packages are often called upon to offer electrical insulation from nearby high voltages and to shield the circuitry inside from electromagnetic radiation.

2.3.5.5.1.1.5 Temperature

Temperature protection is something that packages can provide only briefly due to an external excursion. Temperature is usually thought of as being an important part of the overall environment in which a circuit must function and in which the package must continue to offer protection against all the various other environmental hazards discussed above.

2.3.5.5.1.2 Providing Electrical and Thermal Paths

This is the function that creates many of the difficulties associated with packages. The difficulty comes with the need for allowing continuing uninterrupted communication back and forth between the inside of the package and the outside while providing simultaneously the various types of environmental protection.

2.3.5.5.2 Popular Package Configurations

The extremely wide variety of conditions under which thick film hybrid circuits must function naturally leads to many different physical package configurations. The desire and need for some kind of package uniformity and the common needs of many users has led to extensive use of certain common configurations. The package configurations in use today can be placed in four general categories: (1) TO type, (2) Flatpacks, (3) Dual In-Packages (DIP's), and (4) Other types specials, etc.

2.3.5.5.2.1 TO Configurations

This is the familiar hat-shaped package that has been used extensively for transistor packages. It has a flat metal base through which wires pass (insulated by glass). A thick film multilayer circuit can be attached to the metal base by soldering or attachment with epoxy adhesives.

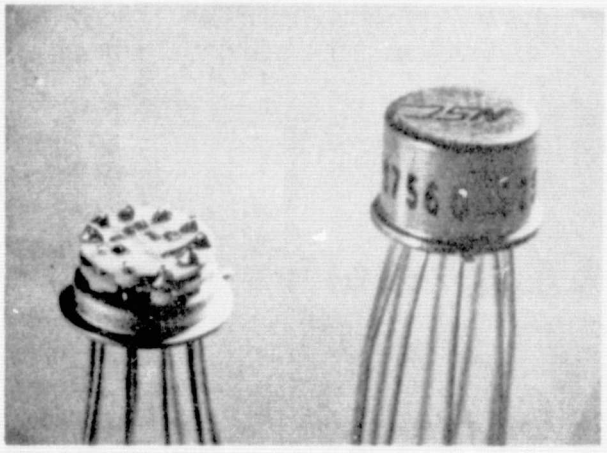


FIGURE 2.3-13 TYPICAL TO PACKAGE WITH SUBSTRATE MOUNTING

2.3.5.5.2.2 Flat Packs - This package configuration has leads that extend horizontally out the sides of the package. For packages with many leads, egress can be on all four sides. The basic construction can be metal, glass, ceramic or plastic.

Where the TO package is usually attached to the printed circuit board by inserting the leads through holes in the PC board and then soldering, the flat-pack is attached by soldering or welding the leads to matching conductor runs on the PC board. No mounting holes on the PC board are needed. Flatpack leads are usually ribbon leads. A common size and spacing is .010 inch leads on .050 inch centers.

Flatpacks come in a wide variety of sizes, ranging from as small as .250 inch square with four leads on each side to over 1.0 inch square with as many as 80 leads. Although they are not as standardized as the TO series where the same package is made by different manufacturers, each package manufacturer

does have several standard sizes to choose from. Standardization of sizes from one manufacturer to the next is a distinct possibility.

Flatpacks allow a large area for circuitry and thus are popular for the more complex circuits. Thick film multilayer circuits can either be mounted on the base of the flatpack and a cover sealed on (much the same way as is done with the TO cans) or the base of the flatpack itself can be the thick film circuit. Flatpacks are, in general, more expensive than other packages.

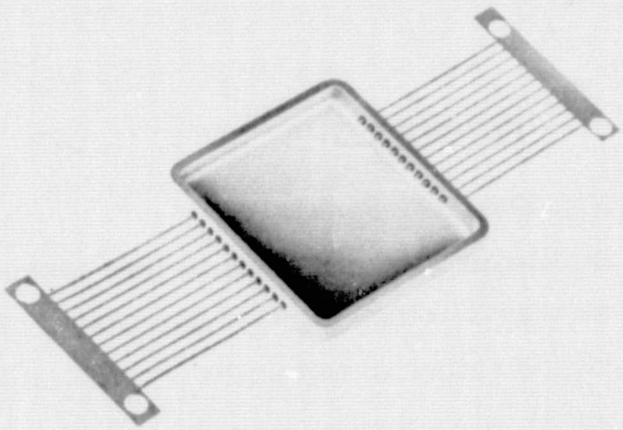


FIGURE 2.3-14 TYPICAL FLATPACK CONFIGURATION

2.3.5.5.2.3 Dual In-Line Packages (DIP's)

The leads of the DIP are arranged on two sides of the base of the package in much the same way as with the flatpack. The most common spacing is 0.1 inch centers. The standard distance between the rows of the leads (after they are bent at right angles) is 0.3 inch or multiples of this spacing. A 14 lead DIP is approximately 0.75 inch long. DIP's come in longer packages with as many as 40 leads.

The leads of the DIP are much sturdier than those of the average flatpack. They are often made from a metal stamping but are of heavier gage. When they are bent at right angles so that the leads point "downward" from the base of the DIP, they are in position to be inserted into a PC board and soldered.

DIP's are commonly made with ceramic bases. The covers may be of ceramic or the package can be encapsulated in plastic. DIP packages are as a general rule, less expensive than flatpacks.

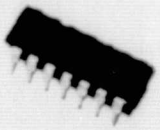


FIGURE 2.3-15 TYPICAL DIP

2.3.5.5.2.4 Non-Standard Packages

Thick film multilayer circuits seem to lend themselves to non-standard packages more so than do other types of integrated circuits. This is partly because of the rugged nature of thick film, which allows use of less expensive and non-conventional packaging approaches. It is also because many applications of thick film multilayers are unique and lead to a variety of package dimensions. The thick film substrate itself is a good start towards fabricating a package. Many thick film applications tend toward high volume situations where it can be economical to build a unique package specifically for the particular circuit rather than use one of the standard configurations.

There are a variety of metal packages that are somewhat non-standard. They have excellent lead-in seals and offer good heat dissipation capability.

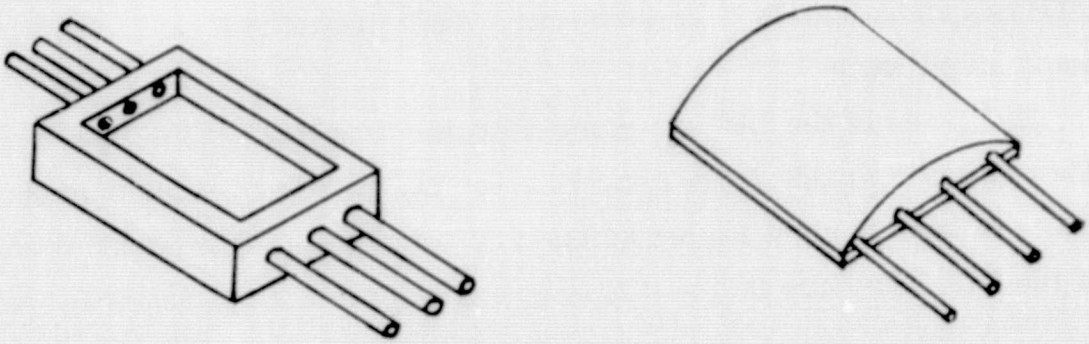


FIGURE 2.3-16 NON-STANDARD PACKAGE

2.3.6 Thick Film Element Design

The thick film element design phase is of course, one of the most important steps in the design of a reliable multilayer ceramic circuit. The conductive interconnect system is that medium which provides a base for mounting the active devices and furnishes the necessary discretionary electrical interconnections. These elements can be segregated into four distinct types; resistors, conductor/dielectric, inductors and capacitors. Each circuit element has its own inherent set of dimensional rules and formulas which may overlap.

2.3.6.1 Resistor Design

As discussed in the Test Pattern Utilization section (2.8), thick film resistors are somewhat difficult to fabricate as a part of complex multilayer circuitry. The multitude of refirings and extensive use of dielectric materials as well as area consumption may sometimes dictate the use of chip resistors.

Before the thick film resistor can be designed and drawn, several factors have to be considered. These include dimensions, clearances, trimming allowances and power rating. In addition, the paste manufacturer's literature should be studied thoroughly in order to determine the relation between resistor material selected and processing parameters for other materials. (See the Materials section on resistors.) Every organization that fabricates microcircuits should generate information on processing conditions for every paste utilized. Up-to-date information should be taken into account prior to planning and layout of thick film resistors.

2.5.6.1.1 Test Pattern Utilization - Refer to resistor Test Pattern Utilization section (2.8) prior to calculating resistors.

2.3.6.1.2 Sheet Resistitivity

Although the sheet resistivity of a particular resistor paste is compounded to a specific value (10 Ω /□ , 100 Ω /□ , 1K Ω/□ etc.) by the paste manufacturer, the final value after firing varies considerably among various fabrication facilities. Factors such as screening condition, paste condition, firing profile, resistor geometry and termination conductor material can have considerable effect on final resistance readings. The basic equation for resistance is:

(1) $R = \frac{\rho \ell}{A}$

Where R = Resistance, ohms
ρ = Bulk resistivity
ℓ = Length of resistor
A = Area of resistor cross-section

Expanding

(2) $R = \frac{\rho \ell}{A} = \frac{\rho \ell}{TW}$

Where T = Thickness
W = Width

(3) Also, the sheet resistance is inversely proportional to the thickness, or

$\rho_s = \frac{\rho}{T}$ or $T = \frac{\rho}{\rho s}$

Where ρ_s = effective sheet resistivity in ohms/square

Substitution of (3) in (2) provides

$R \text{ (ohms)} = \rho_s \frac{\ell}{W}$

$= \rho_s N$

Where N = number of squares

$N = \frac{R}{\rho s} = \frac{\ell}{W}$

2.3.6.1.3 Power Rating

The normal value for heat dissipation in thick film resistors is 25 watts per square inch of active resistor. The active resistor area is that area of resistor remaining after final trimming operations. The conductor termination areas are not included. The power to be dissipated by a resistor in a circuit may be calculated from:

$$P = I^2 R = EI = E^2/R.$$

The area of a resistor required to dissipate its generated heat may be calculated from the relation that

$$A = \frac{P}{K}$$

where A = resistor area (in^2),
P = power dissipated by resistor (watts), and
K = rated resistor power (watts/sq. in).

Example:

If a resistor is 0.10 inches long and 0.025 inches wide and manufactured with paste that has a power handling capability of 25 watts/in^2, then the maximum power that the resistor can dissipate is

$$P = A \times K \times T_c$$

$$= (0.10 \times 0.025) \times 25 \times 75 \text{ percent}$$

$$= 0.039 \text{ watt}$$

where

A = area in in^2

K = power rating in watts/in^2 (thick film paste), and

T_c = trimming correction (percent material remaining after trimming).

If the area is known, the power that a resistor can dissipate can be readily calculated from

$$P = A \times K.$$

When determining the minimum width for a resistor with a specified power rating, the following may be used

$$Wm = \frac{(\rho_s P)^{\frac{1}{2}}}{KR}$$

Where Wm = the minimum width in inches of active resistor (must exceed .020 inch)

ρ_s = sheet resistivity of paste (determined by "as fired" resistor monitors)

R = resistance required, and

K = rated resistor power.

2.3.6.1.4 Allowance for Trimming

Thick film resistors can be screened and fired to an accuracy of approximately 10 to 25 percent. If closer tolerances are required, it is necessary to trim the resistor by either an air abrasive or laser technique. It is standard practice to choose the size of a resistor so that its value is approximately 75 percent of the desired value. The resistor is then brought to the correct value by trimming.

Example:

If the final circuit value of a resistor is to be 20 kΩ, the design value of the resistor should be

$$R = 20k \times 75\% = 15.0\ k\Omega$$

Assuming the sheet resistivity of the ink for the resistor is 10kΩ/sq. the number of squares, N, should be

$$N = \frac{R}{\rho_S} = \frac{15000}{10000} = 1.5 \text{ squares.}$$

If the resistor is .030 inches wide, (.020 inches minimum width was determin i by power calculations) the length will be

$$L = \frac{RW}{\rho_S} \quad \frac{15000 \times .030}{10000}$$

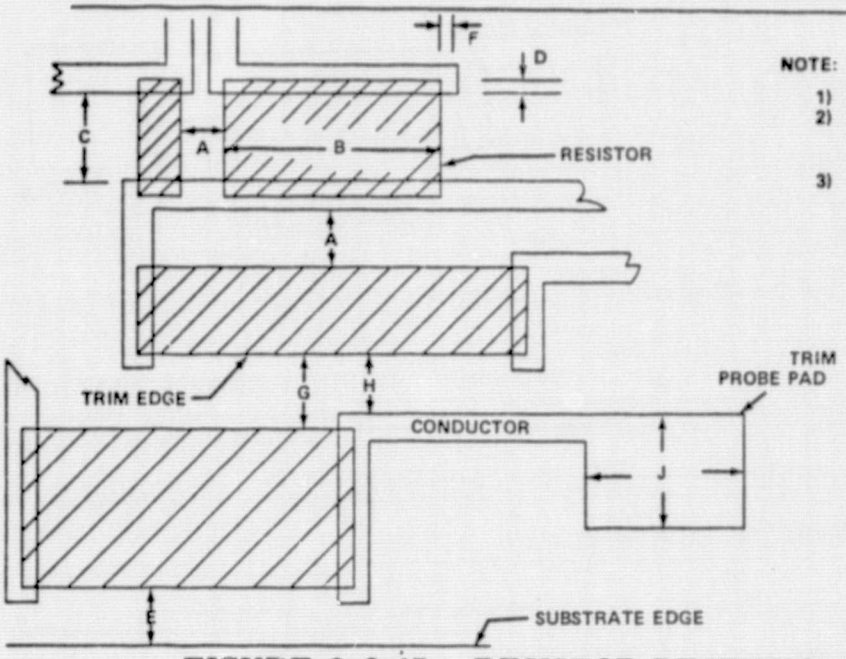
L = .045 inches.

The final value is obtained by trimming (removing) a portion of the resistor material from the substrate. This has the effect of increasing the number of squares and thus the resistance.

2.3.6.1.5 Resistor Layout Dimensions

The resistor layout dimensions and clearances are shown in Figure 2.3-17. One side of each resistor must have a trim edge.

	A	B	C	D	E	F	G	H	J
Preferred	.020	.040	.040	.010	.030	.004	.030	.025	.030
Minimum	.015	.020	.025	.005	.015	.000	.020	.015	.015



NOTE:
1) DIMENSIONS IN INCHES
2) G AND H DIMENSIONS ARE FOR LASER TRIMMING. INCREASE DIMENSIONS G AND H BY .010 FOR ABRASIVE TRIMMING.
3) LENGTH OF RESISTOR (C) IS ALWAYS BASED ON THE DIMENSION BETWEEN CONTACT PADS

FIGURE 2.3-17. RESISTOR DIMENSIONS AND CLEARANCES FOR TRIMMING

2.3.6.1.6 The number of resistor inks per substrate should be kept to a minimum. Each resistor ink requires separate artwork, its own screen and a separate screening operation.

2.3.6.1.7 Orient resistors parallel to X or Y axis for processing repeatability and ease of trimming.

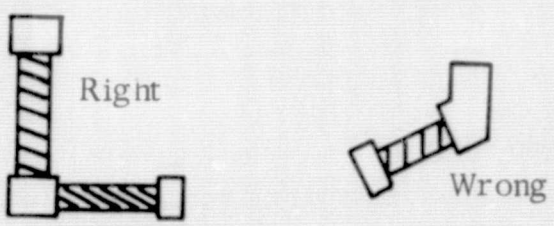


FIGURE 2.3-18

2.3.6.1.7 Avoid zig-zag or meander resistor configurations. Hot spots may be created at corners. Zig-zag resistors are also difficult to trim.

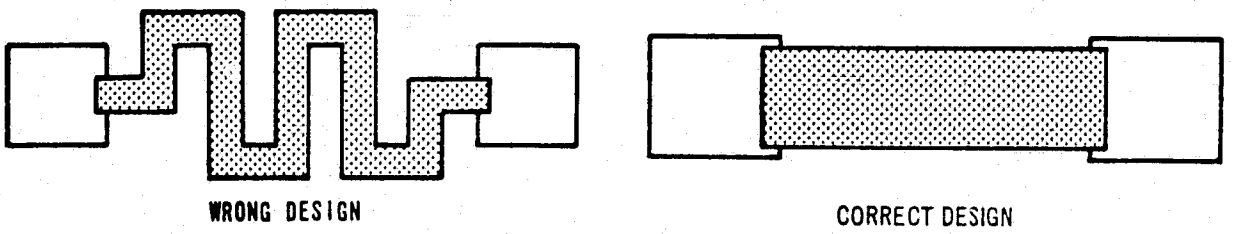


FIGURE 2.3-19

2.3.6.1.8 Avoid closed loops, single closed path resistors cannot be trimmed and measured. The proper layout procedure when a closed loop required is to incorporate a break in the conductor path to fabricate resistor processing with loop to be closed by a jumper at assembly.

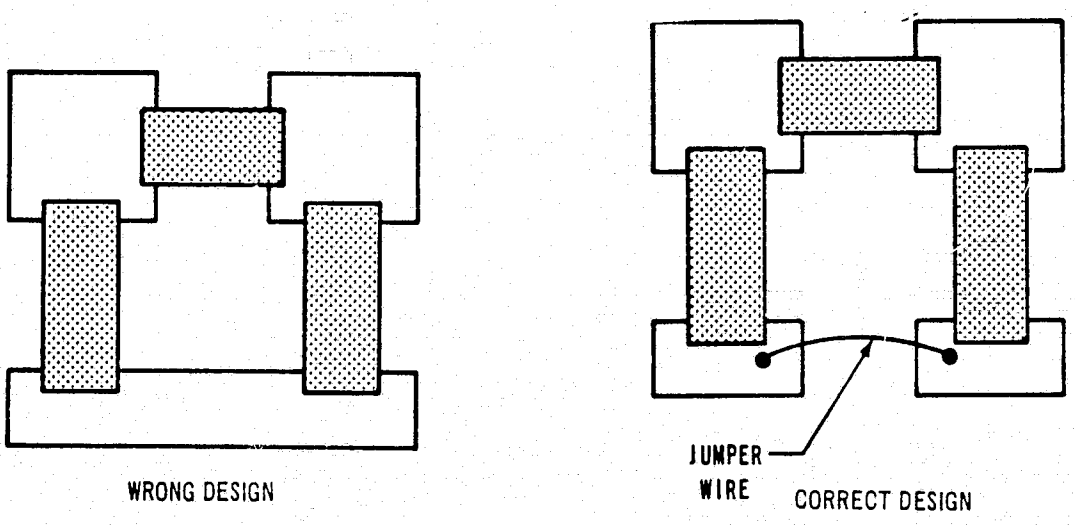


FIGURE 2.3-20

2.3.6.1.9 Resistor Aspect Ratio

The aspect ratio of a film resistor is the ratio of its length to its width, or $\frac{L}{W}$. This is also equal to the number of squares, N, in the resistor. For resistor design where the length is greater than the width, the maximum aspect ratio should not exceed 10:1. For good design, it should be 5:1 or less.

When the width must be greater than the length, the aspect ratio should at least be 1:5 and never more than 1:10. Resistor geometries should be kept as close to the test pattern configurations as possible.

It is again emphasized that data such as design curves are established by the paste manufacturer and the processing laboratory. The designer should use such information to gain greater layout flexibility. For example, if a resistor length is restricted on the substrate due to other considerations, the data obtained by test pattern utilization would indicate the choice of paste resistivity to be used.

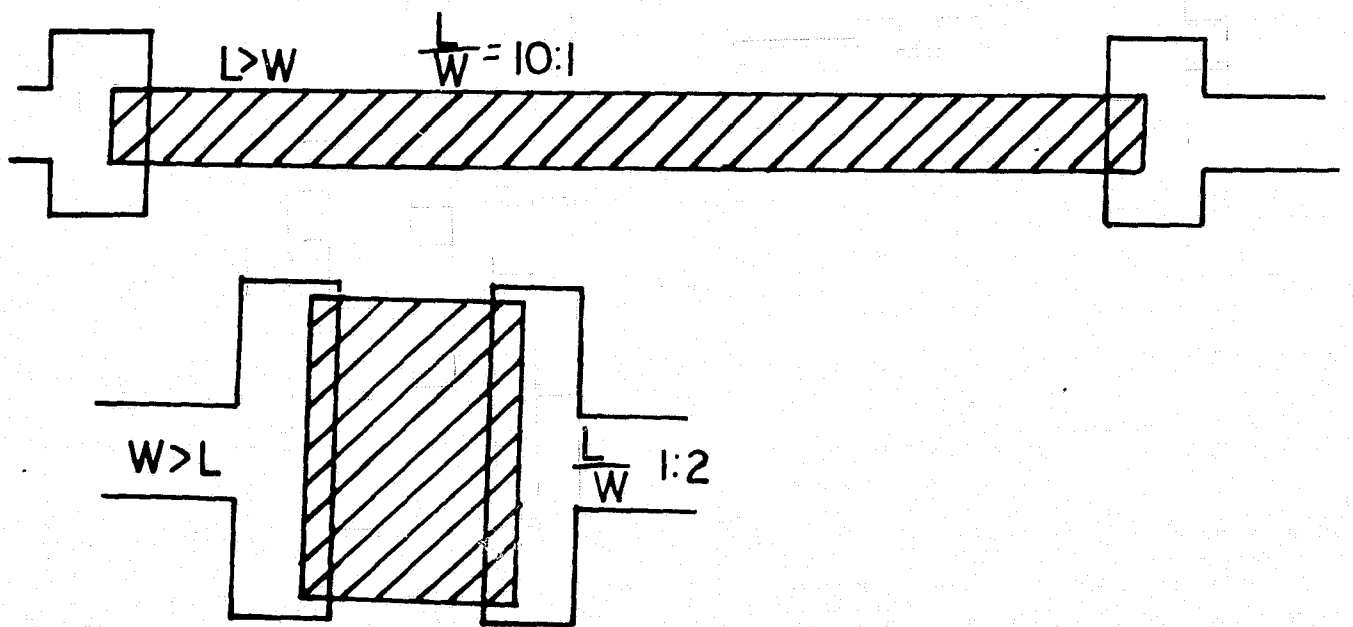


FIGURE 2.3-21 - SHOWS A THICK-FILM RESISTOR PROCESS CONTROL SHEET CURRENTLY IN USE AT ECI

THICK FILM RESISTOR SHEET

TITLE:_____ DATE_____ CIRCUIT NO._____ REV___

REF. DES.	NOMINAL VALUE	TOL	PWR WATTS	DESIGN VALUE	RESISTOR RANGE		WIDTH	LENGTH	NOMINAL SHEET RESISTIVITY Ω/□	CALCULATED SHEET RESISTIVITY Ω/□	TERM. COND. MATL.
					MIN	MAX					

NOTES:

SHEET _OF_

2.3.6.2 Conductor/Dielectric Design

The conductor dielectric interconnect system is an extremely important element in the multilayer circuit design. A poor design can result in a high incidence of shorts and/or opens in the circuitry during processing. A poor design can also result in excessive assembly costs as well as reduced final circuit reliability. As is the case with the other thick film elements, the final circuit configuration is dependent on the processing expertise and the capabilities and limitations of the materials used (see Test Pattern Utilization and Materials section).

The dimensions shown are for gold fine line conductors and crystalizable dielectrics unless otherwise specified.

2.3.6.2.1 First Conductor Layer

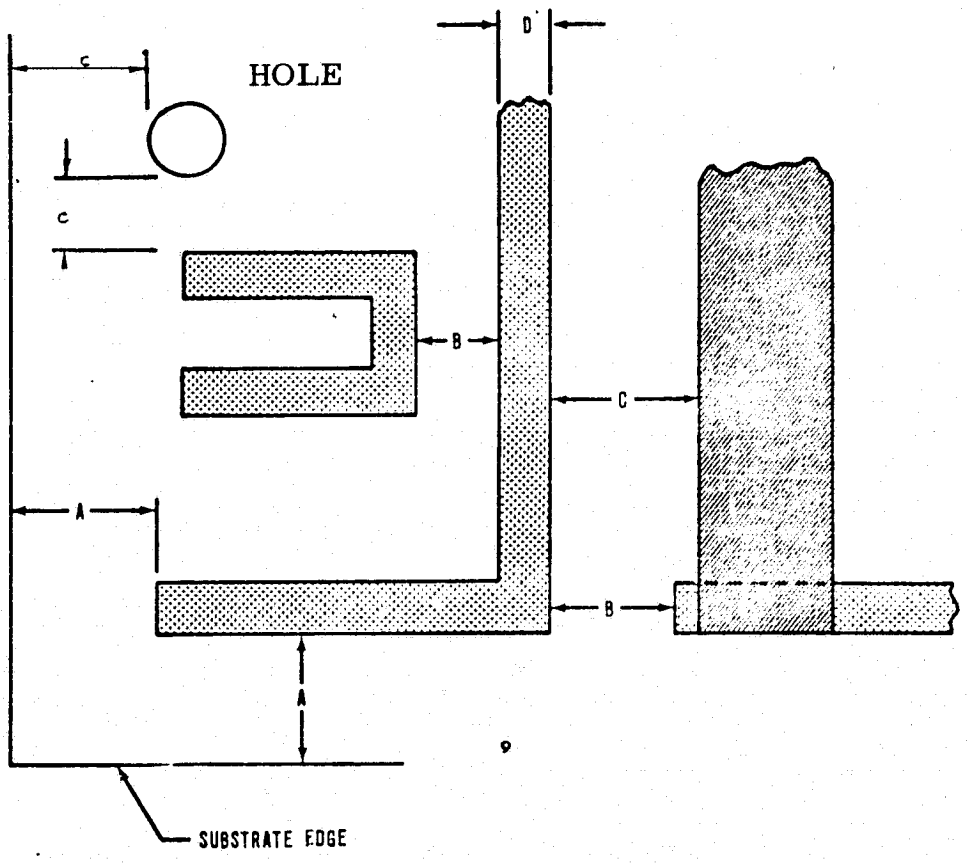
Figure 2.3-22 gives requirements for the first conductor layer. Maximum line widths are not specified since this parameter is sometimes dictated by special power and voltage requirements. However, an unnecessary amount of conductor material should be avoided, especially in multilayer construction. As stated before, conductor lines and resistors should run parallel to the X and Y axis.

2.3.6.2.2 Conductor Terminal Design

Do not run conductors around the edge of the substrate. Edge printing requires special tooling and reduces yield (Figure 2.3-23).

2.3.6.2.3 Beam Lead Device Mounting Pads.

Beam lead discrete devices typically require narrow (0.005 inch) conductor interconnect lines with spacings of 0.005 inch. The beam lead device must normally be placed on the substrate or first layer. The conductor lines that make contact with the leads are flared (expanded) once outside the device's dimensional areas as shown below. Fine lines and spacings are difficult to process and therefore yields are improved with broader conductor lines and spacings.



DIMENSION	A	B	C	D[1]
PREFERRED	.025	.010	.020	.010
MINIMUM	.010	.005	.015	.005

CONDUCTOR

RESISTOR

NOTES:

1. Exceptions must be made for conductor pads for beam lead devices.
2. Dimensions in inches
3. Resistors may be post or pre-terminated depending on materials used.

FIGURE 2.3-22 FIRST CONDUCTOR LAYER

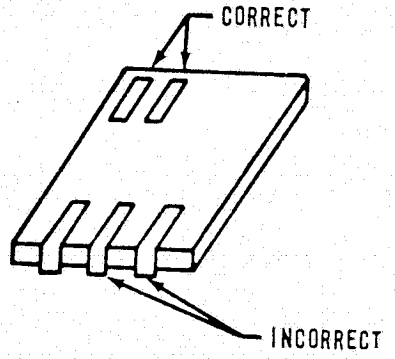
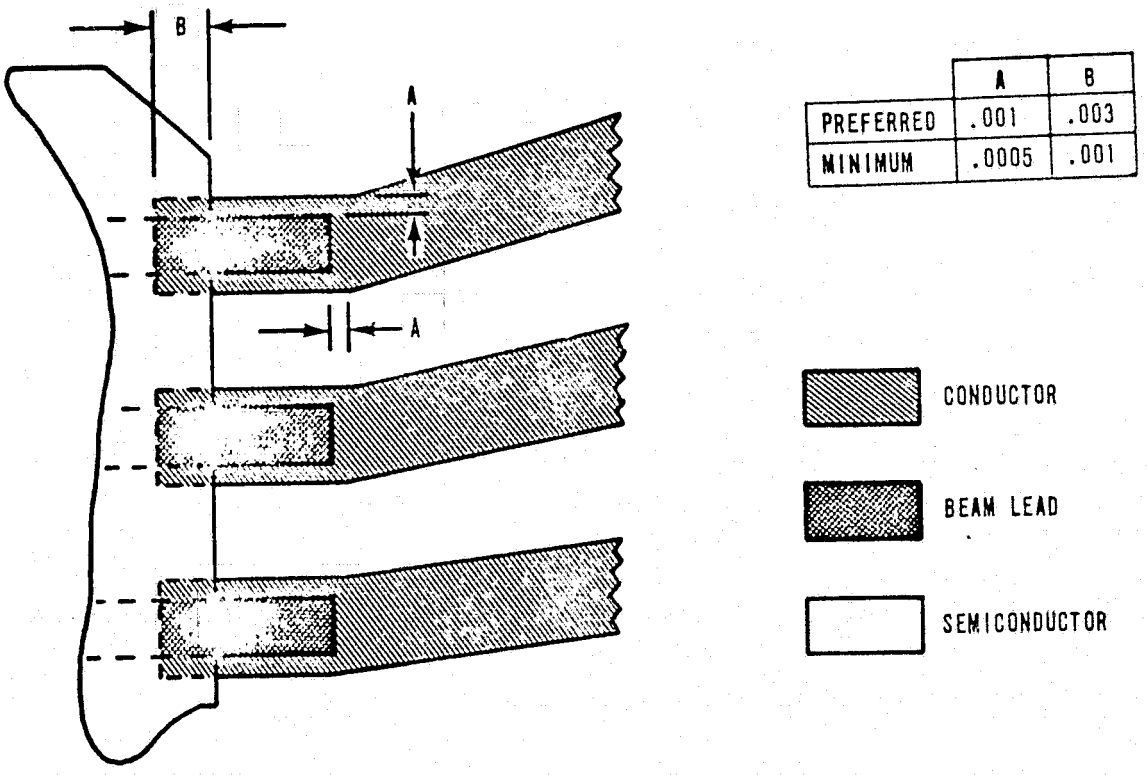


FIGURE 2.3-23 CONDUCTOR TERMINAL DESIGN



	A	B
PREFERRED	.001	.003
MINIMUM	.0005	.001

FIGURE 2.3-24 BEAM LEAD CONDUCTOR LINE DESIGN
(Dimensions in inches)

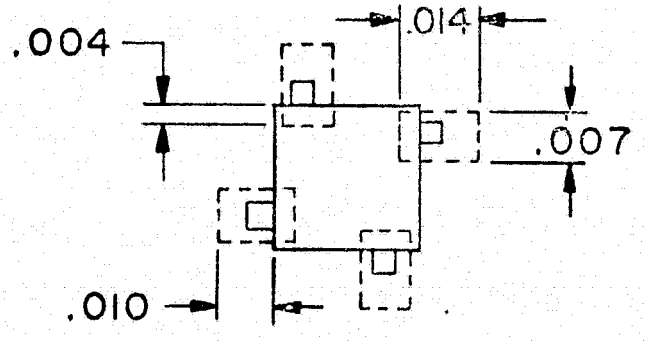
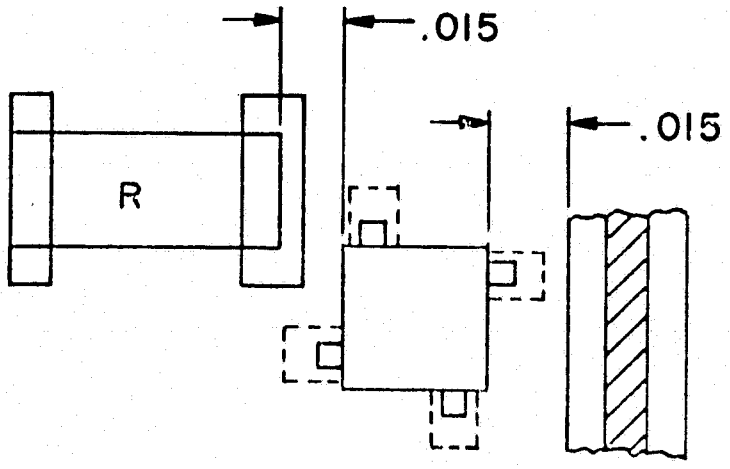


FIGURE 2.3-25 BEAM LEAD PADS (one per side)

A second layer shall be a minimum of .015 inches from the body of beam lead devices.



NOTES:
1. Flair out lines and spaces to normal widths in minimum length.
2. Dimensions in inches

FIGURE 2.3-26 BEAM LEAD CONDUCTOR LINE DESIGN

2.3.6.2.3.1 General Rules Beam Lead Devices

1. Conductor leads to all beams of each beam lead device must be on the same conductor level.
2. No metallization should cross under a beam lead device.
3. Conductor overlaps should not occur in the beam lead bonding area.

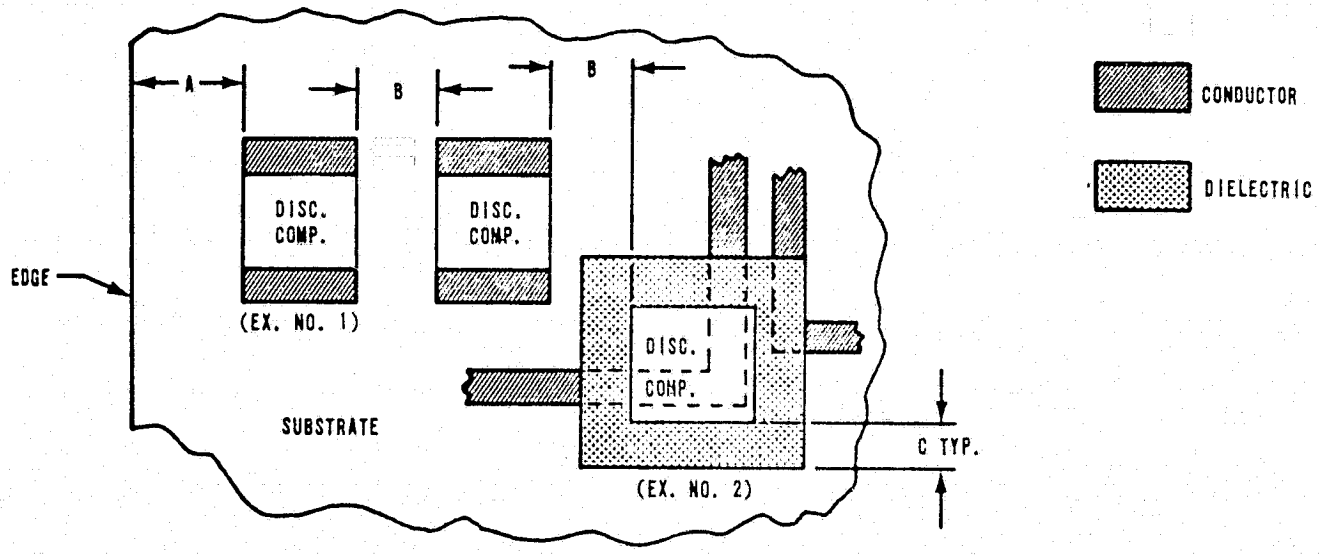
2.3.6.2.4 Discrete Component Mounting Rules

Several methods are available for mounting discrete components on the substrate and are as follows:

1. Bonding of chip or die on the base with a nonconductive adhesive with electrical connections made by thermocompression wire bonding.
2. Direct die attachment.

3. Direct die chip attachment using solder or metal preforms.
4. Bonding of components on the base with a conductive adhesive.
5. Direct thermocompression bonding using beam lead devices.

Figure 2.3-27 illustrates the mounting clearance for discrete components using a non-conductive adhesive. Example 1 shows discrete components placed directly on the substrate while Example 2 shows a component (semiconductor chip, capacitor, etc.) placed over two or more metal conductor lines.



	A	B	C
PREFERRED	.030	.024	NOTE 1
MINIMUM	.020	.020	—

NOTE:
1. ALLOW .010 AROUND DISCRETE PART AND DRAW TO NEAREST GRID LINE.
2. DIMENSIONS IN INCHES.

FIGURE 2.3-27. DISCRETE COMPONENT PLACEMENT AND INSULATION

2.3.6.2.5 Insulated Components Over Conductors

Figure 2.3-28 shows the proper method of placing base insulated components over a single conductor line using a non-conductive adhesive. A thick-film dielectric insulating layer is required when two or more conductor lines are beneath the component.

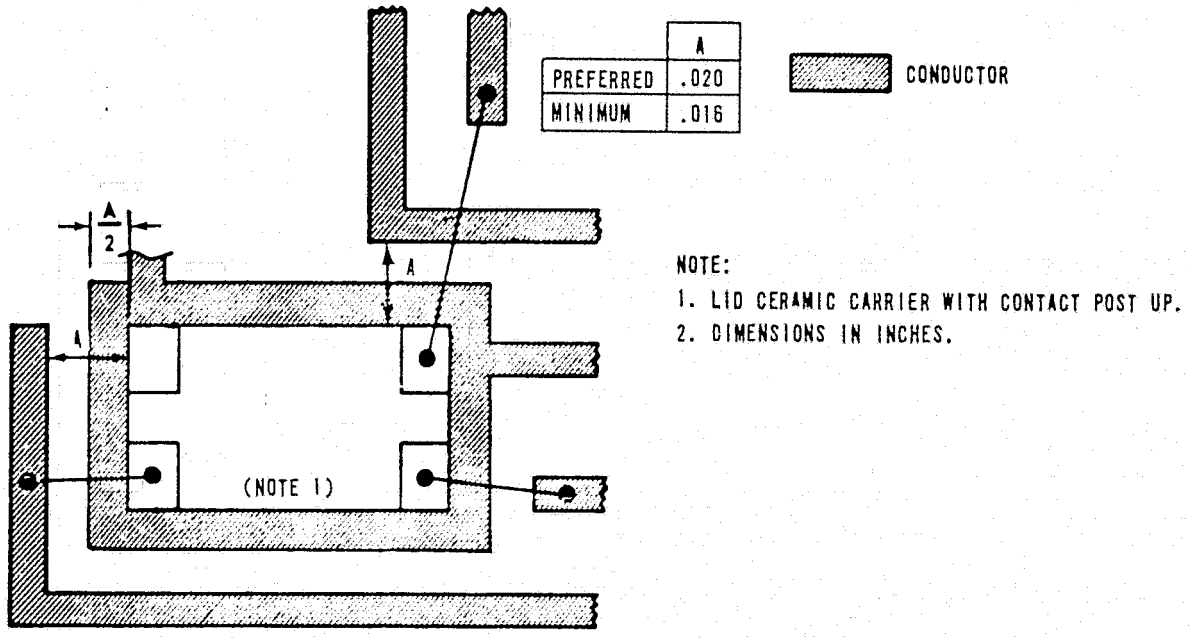


FIGURE 2.3-28 INSULATED COMPONENTS OVER A CONDUCTOR LINE

2.3.6.2.6 Chip Mounting

Figure 2.3-29 shows the method by which a semiconductor chip may be bonded directly to metallized pads or lines (direct die attachment method).

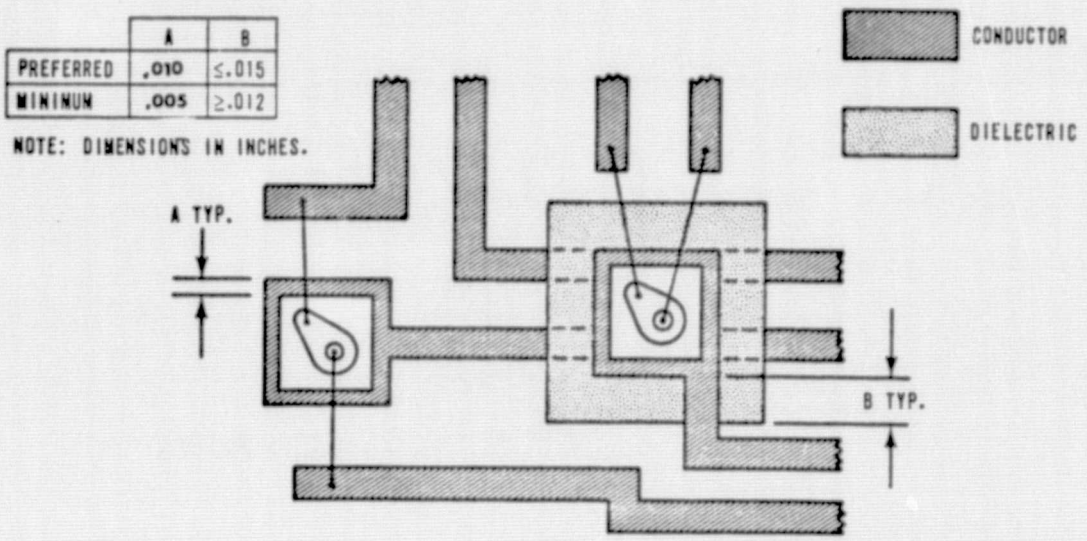


FIGURE 2.3-29 PADS FOR MOUNTING SEMICONDUCTOR CHIPS

2.3.6.2.7 Chip pad wire bonding to be .010 inches minimum from chip.

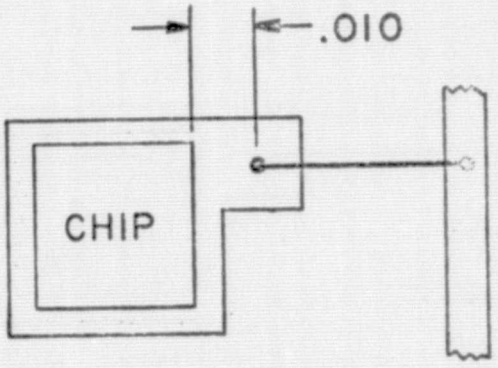


FIGURE 2.3-30

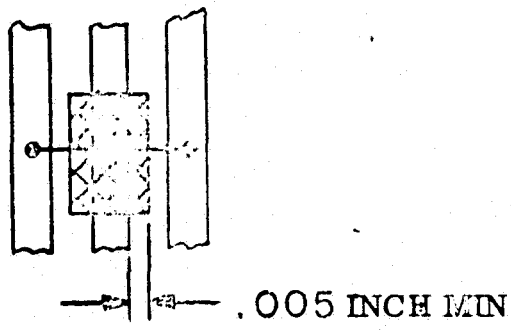


FIGURE 2.3-31 Insulation used to prevent shorting of wire when crossing a conductor shall overlap isolated conductor by .005 inches minimum.

2.3.6.2.8 Capacitor termination clearance under capacitor to be .015 inches minimum.

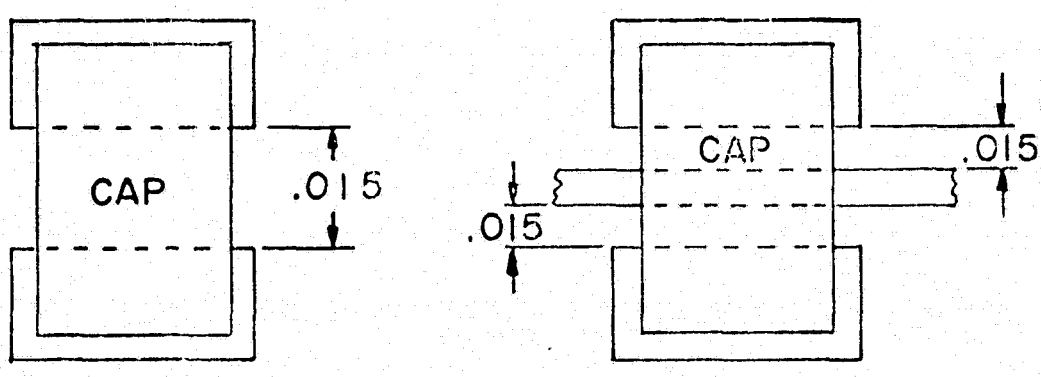
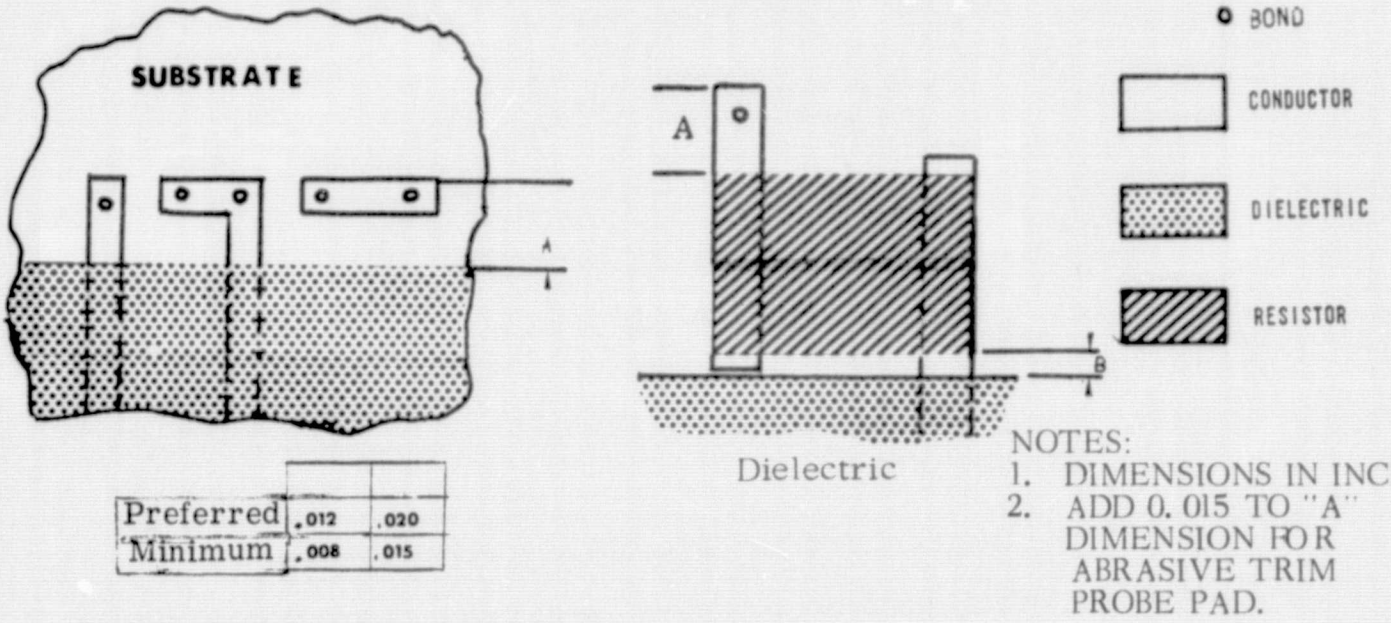


FIGURE 2.3-32

Caution: Leads under capacitors to be no thicker than capacitor end terminations. (Dimensions in inches.)

2.3.6.2.9 Bond Pad and Resistor Clearances

Bond pad clearances are shown in Figure 2.



Preferred	.012	.020
Minimum	.008	.015

FIGURE 2.3-33. CLEARANCE OF BOND PADS FROM OTHER MATERIALS

2.3.6.2.10 Clearance for Bond Pads Adjacent to Discrete Parts and Other Vertical Obstructions

Chip and wire bonds are .035 inches minimum from capacitors.

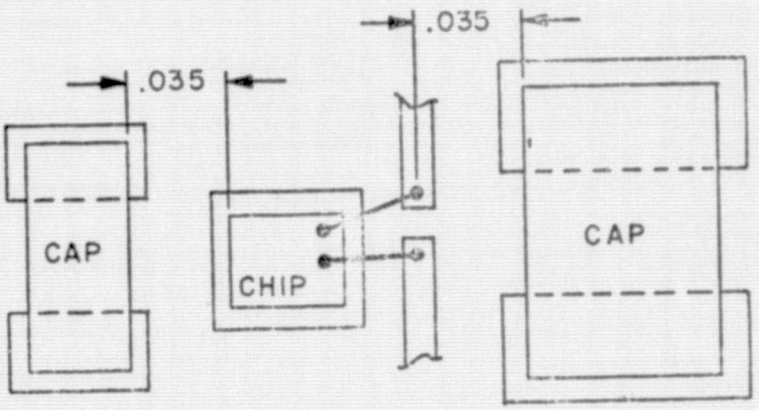


FIGURE 2.3-34

2.3.6.2.11 Capacitor mounting pads will be larger than the capacitor by .005 inches on each side and .010 inches on each end for solder or conductive epoxy bonding.

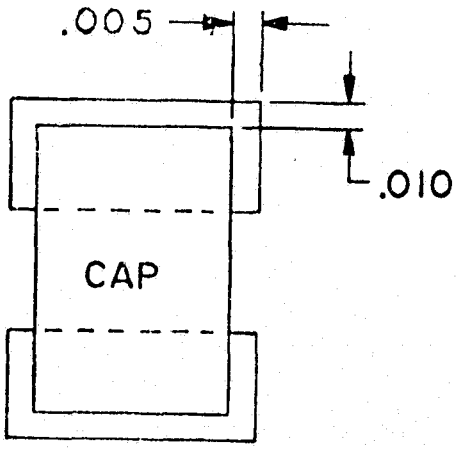
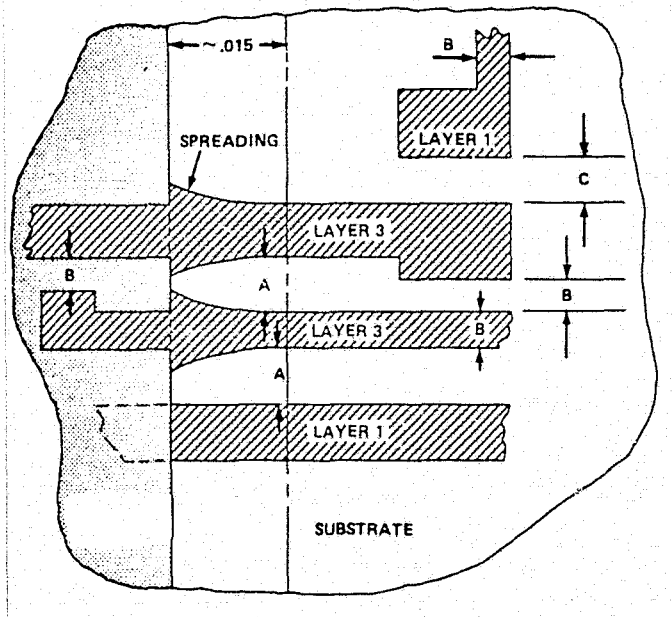
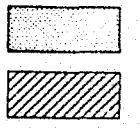


FIGURE 2.3-35

2.3.6.2.12 Multilayer Conductor Separation on Substrate Base

Most thick film conductor materials spread as they are printed across a dielectric edge. This occurs within .015 inch of the edge and therefore, must be considered in design tolerance between conductors as shown in Figure 2.





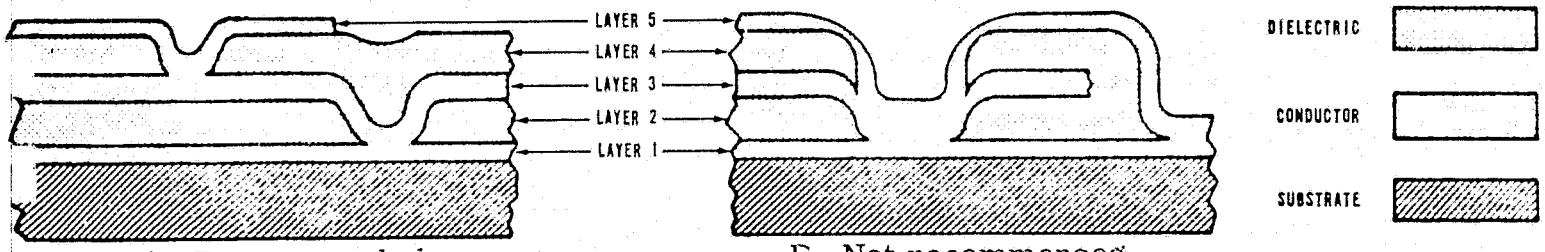
NOTE: DIMENSIONS IN INCHES

	A	B	C
PREFERRED	.020	.010	012
MINIMUM	.015	.005	.005

FIGURE 2.3-36. MULTILAYER CONDUCTOR SEPARATIONS ON SUBSTRATE BASE

2.3.6.2.13 Multilevel Feedthrough Design

Multilayer feedthrough metallization may be required to connect conductor lines through two or more dielectric layers. Because of the difference in thickness of the screened metal and dielectric lines, the windows become depressed when placed directly on top of the other. The recommended practice is to stagger the through connections to minimize this effect.



A. Recommended B. Not recommended

FIGURE 2.3-37. SIDE VIEWS OF MULTILAYER FEEDTHROUGH CONNECTIONS

2.3.6.2.14 Conductor clearance required around window areas are .010 inches minimum.

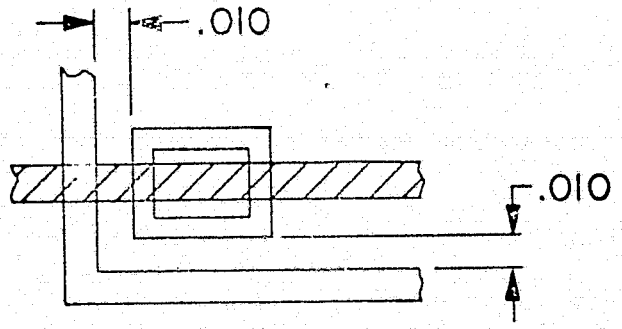


FIGURE 2.3-38

2.3.6.2.15 Insulation planes require a .015 inch square window opening for wire bonding.

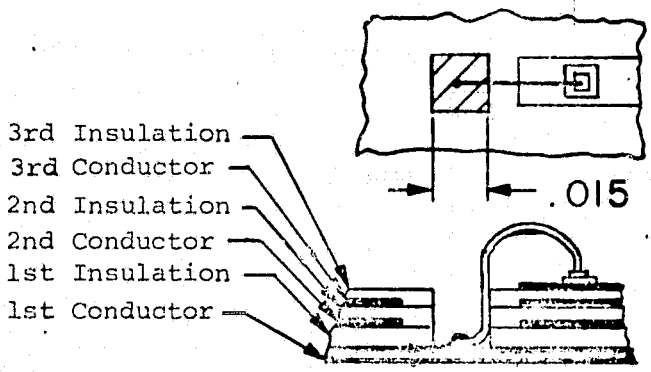


FIGURE 2.3-39

2.3.6.2.16 Single layer insulation to be staggered .020 inches for conductor crossover interconnections where practical to prevent shorting.

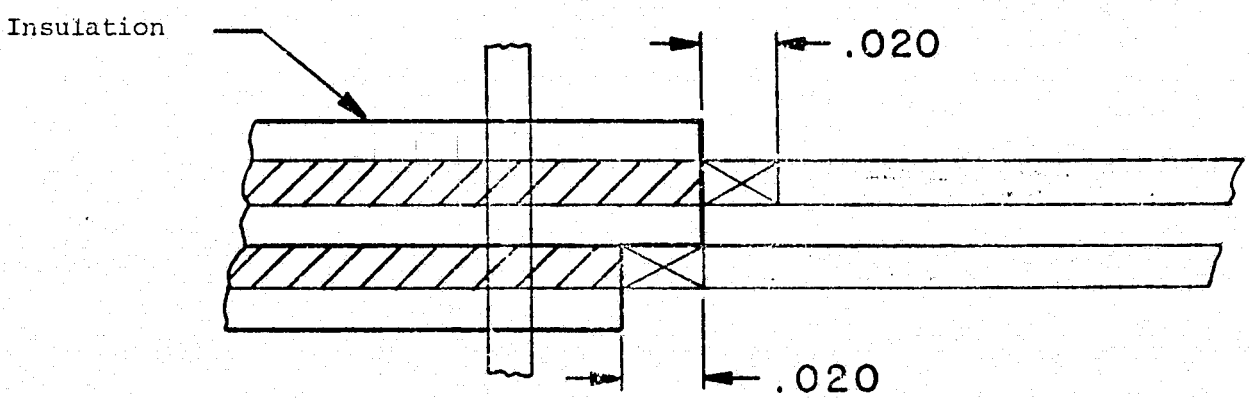


FIGURE 2.3-40

2.3.6.2.17 Dielectric Clearance and Conductor Isolation

As a practical rule, the maximum capacitance of a right angle crossover of two 0.008 inch conductor lines in two adjacent layers is approximately 0.2 picofarad. Dielectric clearance and conduction isolation are shown in Figure 2.3-41 . This method of conductor isolation is used when a small number of conductor crossovers are required.

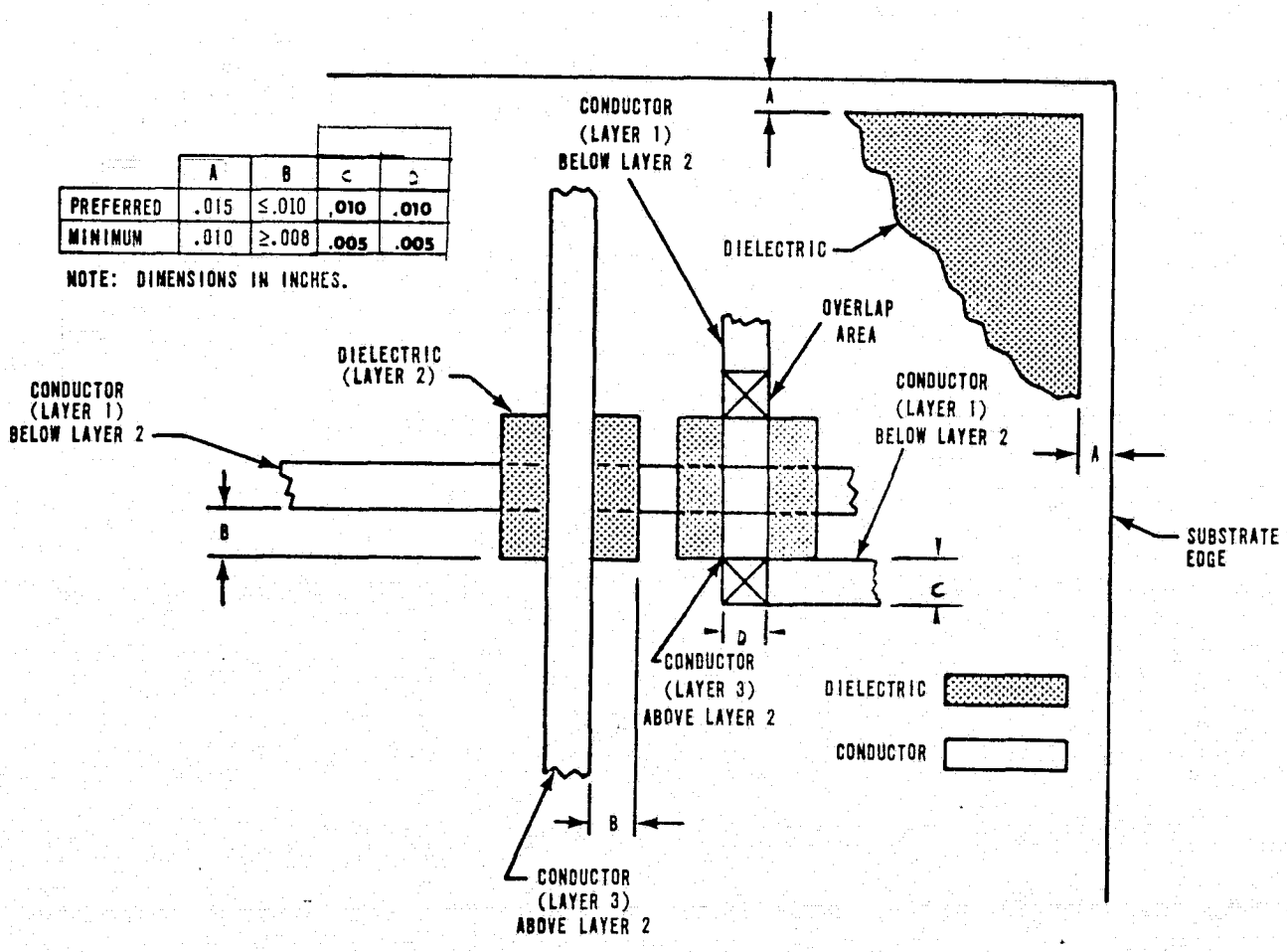
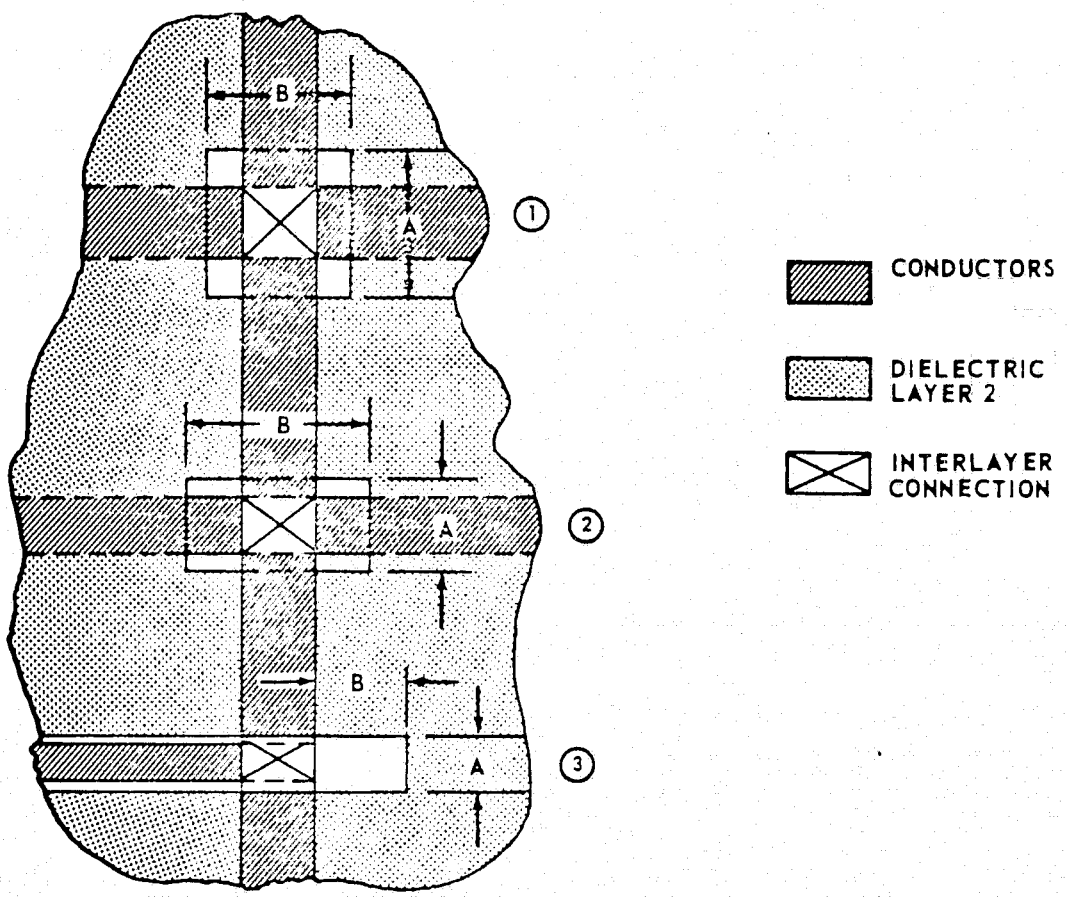


FIGURE 2.3-41 . DIELECTRIC CLEARANCE AND CONDUCTOR ISOLATION

2.3.6.2.18 Dielectric Windows

Vias or windows must be designed in a dielectric layer when making connections between two metal conductor layers. Considerations for these windows are shown in Figure 2.3-42 . These dimensions are determined by material characteristics. Refer to the Test Pattern section (2.8) and Materials section (2.7)



	CASE 1	CASE 2	CASE 3
	A X B	A X B	A X B
PREF.	.020 X .020	.016 X .024	.012 X .012
MIN.	.016 X .016	.012 X .024	.012 X .008

NOTE: DIMENSIONS IN INCHES

FIGURE 2.3-42. DIELECTRIC WINDOW

2.3.6.2.19 Dielectric Window Clearance for Beam Lead Bonding

A clearance must be provided around beam lead devices to prevent damage to devices during bonding.

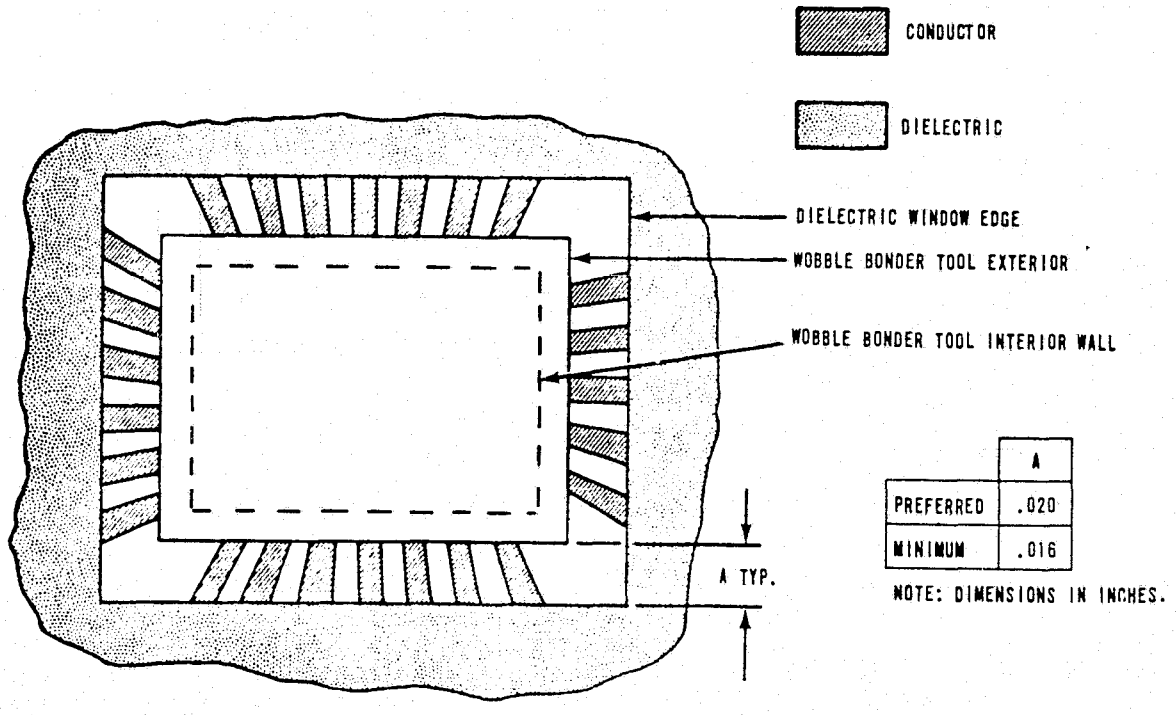
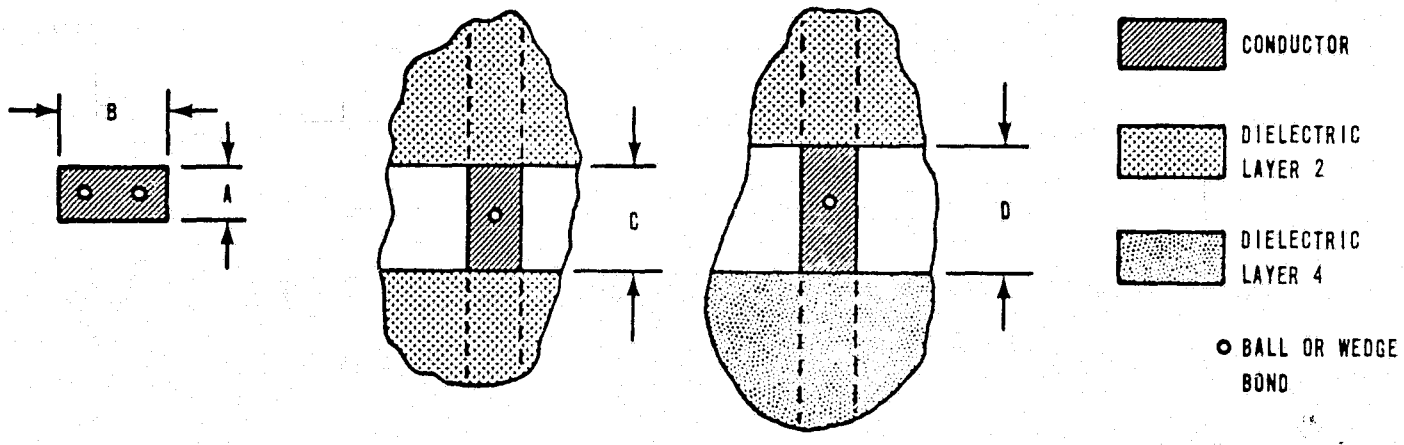


FIGURE 2.3-43. DIELECTRIC WINDOW CLEARANCE FOR BEAM LEAD BONDING

2.5.6.2.10 Bond Pad Dimensions

Bond pad dimensions are shown in Figure 2.3-44. Restrictions are placed due to dielectric intrusion into bonding area.



	CASE 1	CASE 2		
	A x B	A x B	C	D
PREFERRED	.010 X .024	.015 X .020	.024	.028
MINIMUM	.008 X .020	.010 X .015	.020	.024

NOTE:
1. ADD .008 X .008 MIN. AREA FOR EACH ADDITIONAL BOND ON A PAD.
2. DIMENSIONS IN INCHES.

FIGURE 2.3-44. BOND PAD DIMENSIONS

2.3.6.3 Inductor Design

Thick film inductors can be achieved by depositing either spiral or linear patterns of conductor ink on the substrate. Solder coating can increase the conductivity so as to improve the Q of the deposited inductor. Inductance values as great as 250 pH can be obtained at UHF frequencies. However, practical constraints imposed by the high packaging density of hybrid microcircuits may seriously limit the range of inductances possible as well as the quality of the inductors.

Two typical configurations are used for deposited spiral inductors; one is circular, the other square, as shown in Figure 2.3-45.

In Figure 2.3-46, the inductance for these coils is given by:

(1) $$L = \frac{0.8\, a^2\, n^2}{6a + 10c} \times 10^{-3}$$

for circular coils, and

(2) $$L = 85 \times 10^{-4} \times S \left(\tfrac{1}{2} \times n\ (5/3)\right.$$

for square coils,

where n = number of turns, a = mean radius = (OD + ID)/.004 inch, c = depth of winding = (OD - ID)/.002 inch, and s = surface area of coil (cm^2).

The inductance given by these equations is the low frequency value in microhenries; the value obtained is generally accurate to within 5%. The type of substrate used has little effect on the inductance value; however, it does affect the Q and distributed capacity (and therefore the self-resonant frequency). A square coil has a larger inductance than a circular coil of the same ID and OD (probably due to the greater length of conductor involved) and is far easier to lay out and produce. For these reasons, the square configuration was more commonly used for deposited inductors in the past. With the advent of computers having graphic software, the circular spiral inductor has become more popular recently. The circular spiral has the advantage of having a higher Q for a given inductance value.

The following discussion is limited to the square spiral inductor configuration. The self-resonant frequency is given approximately by:

$$(3) \quad f_o = 43.5 \times 10^8 \times \frac{1}{\epsilon_r^{\frac{1}{2}} S^{\frac{1}{2}} n}$$

where ϵ_r = relative dielectric constant of the substrate. As the operating frequency of the coil approaches f_o the apparent inductance La increases toward infinity:

$$(4) \quad L_a = \frac{L}{1 - |f/f_o|^2}$$

The quality factor Q_o measured at $f_o/4$ is given by:

$$(5) \quad Q_o = 3.6 \frac{W}{\epsilon_r^{\frac{1}{2}} \rho n^{4/3}} = 0.57 \frac{S^{2/3} W}{\epsilon_r^{\frac{1}{2}} \epsilon \rho^{4/3}}$$

where W = thickness of the conducting spiral (cm), = resistivity of the conducting material (cm), = resistivity of the conducting material (ohm - cm), p = coil conductor with (cm), and q = conductor spacing (cm) assuming p = q.

Q at an operating frequency other than $f_o/4$ is given by:

$$(6) \quad Q = 4 \times f/f_o \times Q_o$$

It is thus apparent from the equation for Q_o why solder coating the conducting material in spiral coil improves the quality factor. In practice, the Q is usually somewhat lower than predicted. This is generally attributed to increased resistivity of the conducting material due to surface roughness and the strong electric field along the edges of the conductor.

It is not immediately obvious from the equations whether the deposited spiral inductor will yield values of L, Q and f_o which are suitable for high frequency applications. Moreover, assuming the parameter values are acceptable, the question arises: Is the size compatible with hybrid microcircuits? A few illustrative examples should help clarify this point.

Figure 2.3-46 shows inductance and self-resonant frequency as a function of number of turns (spirals) for 0.2, 0.3, and 0.4 inch squares. Inductors physically larger than described by these dimensions, it is felt, are not practical for use in microcircuits. Figure 2-3-47 is a plot of quality factor, Q_o

measured at $f_o/4$. A substrate with $\epsilon_r = 9$, a line thickness, W, of 0.5 mils and a resistivity of 0.01 ohms/square (1.27×10^{-5} ohm-cm for W = .5 mils) is assumed. The conductor width and spacing are equal (p = q) for all cases. The following conclusions may be derived from the curves: (1) Within the size constraints imposed, only inductors of less than approximately 0.4 μh may be realized if a self-resonant frequency of greater than 500 MHz is required; and (2) inductances with large numbers of turns are not consistent with high Q circuits.

Some improvements in the plotted values may be achieved. For example, if a glaze is deposited between the substrate and conductor, the value of ϵ_r will be reduced from approximately 9 to 6, thus improving somewhat the Q and f. Also, by allowing p to decrease (q increase) while n and S remain the same the value of L will increase. These techniques may modify the values shown, but really significant improvements should not be expected.

The inductance value can be increased two to four times and the stray magnetic field can be reduced by placing the spiral between ferrite material. However, this technique raises significant fabrication questions such as: (1) How do you deposit a layer of ferrite material under the spiral? (2) How do you mount a layer above the coil without exerting pressure on the ferrite, thus distorting its electrical characteristics?

So it seems that except for special cases, the advantages of deposited inductances (cost and ease of fabrication) are offset by the following limitations: (1) Inherent low inductances when limited to small physical size; (2) relatively low Q and, in most cases, low self-resonant frequency. However, at UHF frequencies and above, the required inductance values are reasonably low enough to make printed inductors a desirable method for hybrids.

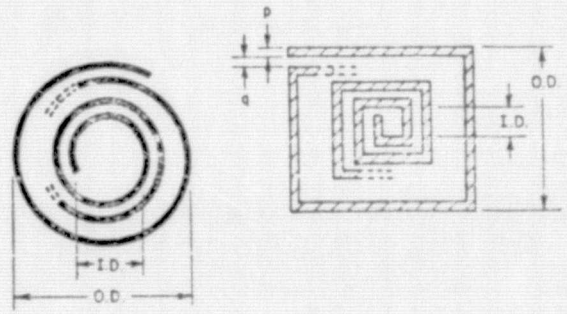


FIGURE 2.3-45

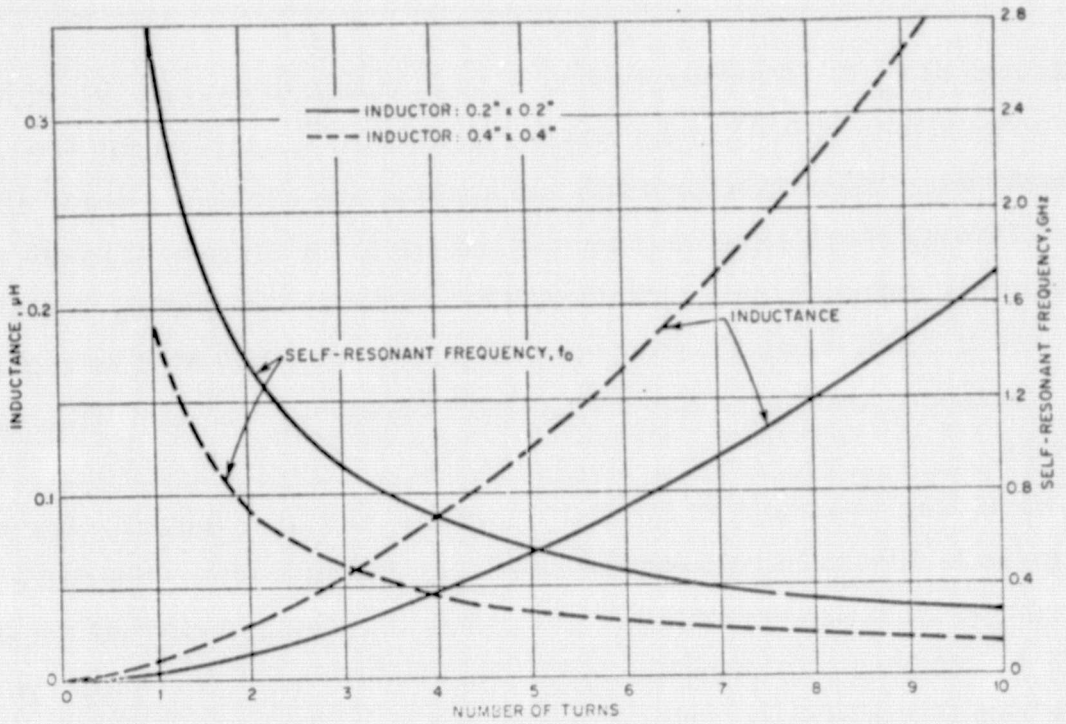


FIGURE 2.3-46 . INDUCTANCE AND SELF-RESONANT FREQUENCY AS A FUNCTION OF THE NUMBER OF TURNS

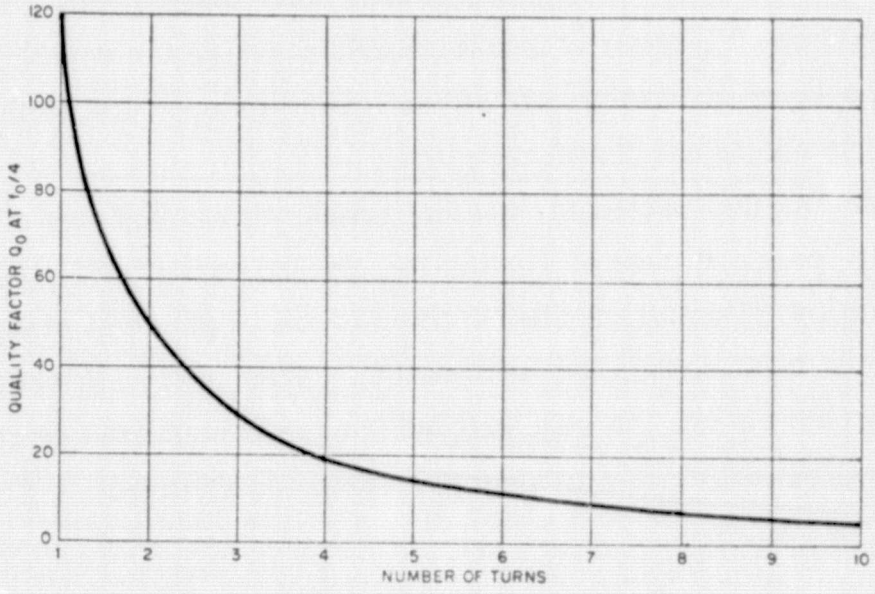


FIGURE 2.3-47. QUALITY FACTOR AS A FUNCTION OF THE NUMBER OF TURNS

2.3.6.4 Capacitor Design

As stated in the Component Selection section, (2.3.5) single layer capacitors whether in chip form or as a substrate element are extremely inefficient in relation to substrate area consumption. Low values of capacitors may be utilized in the design of simple multilayer circuits if the area available permits. The basic capacitance equation is:

$$C = \frac{K\epsilon A\,(N-i)}{t}$$

Where C = Capacitance

ϵ = Constant

A = Area

t = dielectric film thickness

= number of plates (N=2 for calculation)

K = Dielectric constant

Various Units

C	FARADS	uuf	uuf
A	Cm^2	in^2	Cm^2
t	Cm	in	Cm
E	8.854×10^{-14}	.224	.0885

For example, if we wish to calculate the capacitance in micro-microfarads (uuf or pf) with the other units in centimeters (cm), the capacitance equation would be:

$$C = \frac{.0885\ KA}{t}$$

As a practical example, consider a thick film capacitor with an area of .040 $inch^2$. To calculate the capacitance, assume:

Dielectric paste with a dielectric constant of 100 dielectric thickness of .001 inch

$$C = \frac{.224 \times 100 \times .040}{.002} = 448 \text{ uuf}$$

The capacitance per unit area is:

$$C/A = 448/.040 = 11,200 \text{ uuf/inch}^2 = .0112 \text{ uf/inch}^2$$

Based on this example, if a one inch square alumina substrate were used, it would take the entire substrate area to fabricate a capacitor of .01 uf. If only a 1000 pf capacitor is desired, it would take an area of .09 inch square or an area approximately .3 inch on each side.

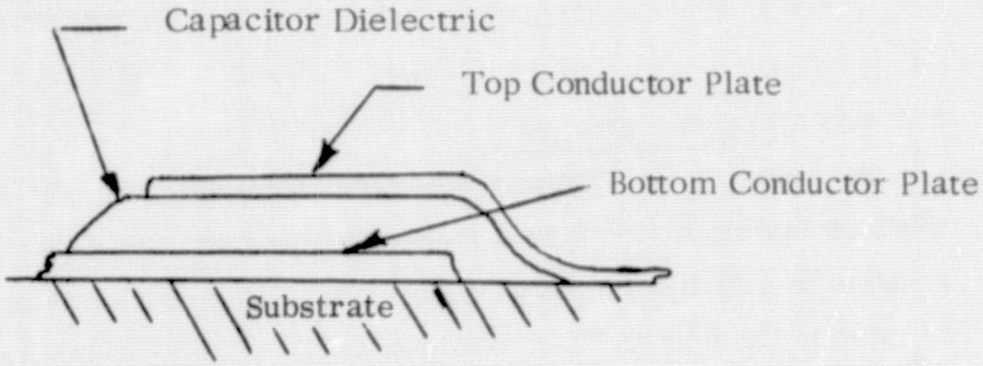


FIGURE 2.3-48
CROSS SECTION OF A TYPICAL THICK FILM CAPACITOR

The active capacitive area is that area where top conductor plate covers the bottom conductor plate separated by dielectric.

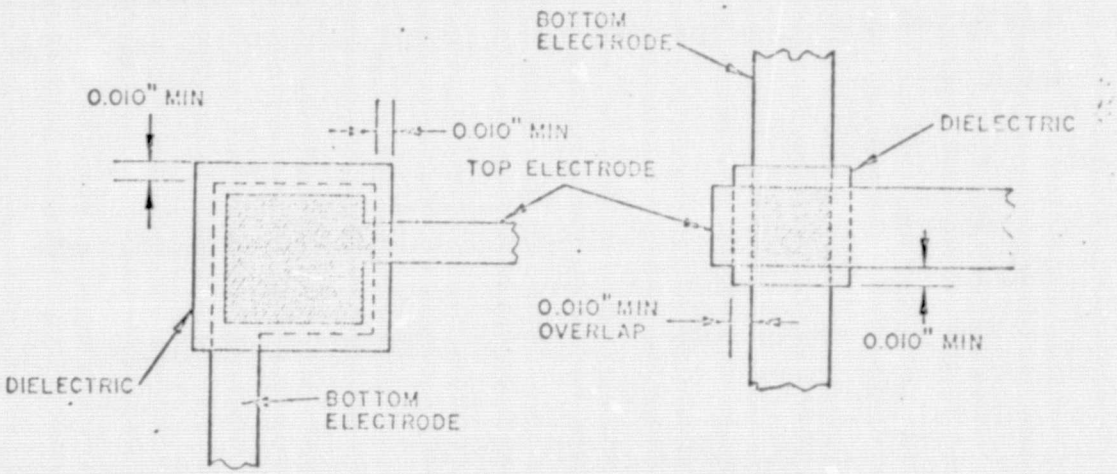


FIGURE 2.3-49. CAPACITOR DESIGN CONFIGURATIONS

ORIGINAL PAGE IS
OF POOR QUALITY

2.3.6.5 Green Tape Ceramic Multilayer Design

The same basic design rules for multilayer ceramic circuitry apply to the green tape method of fabrication. As stated at the beginning of the Design Guide section (2. 3), the major differences between the two substrate systems is the substrate fabrication processes. The inherent shrinkage encountered in the final steps of green tape lamination firing requires very close control of the layout parameters. The final artwork used for fabricating screens and tooling must take this shrinkage factor in account. The percentage of artwork oversize required to compensate for this shrinkage factor must be determined by the processing laboratory responsible for the end product.

The following design parameters are to be used for reference with the understanding that the limitations of the substrate element design are dependent on the expertise and capabilities of the processing labortories.

2.3.6.5.1 Design Parameters

1. The insulating material is a low loss, high strength, preferably 94% Al_2O_3 composition; although, in some cases a 99.5% Al_2O_3 may be used. The insulating layers may be as thin as .0015 inches or as thick as required. Where via holes are involved, it is suggested that the designer consider plane thicknesses of .002 inches or, preferably, .005 inches.

   For other insulating layers, where via holes are not a consideration, preferred thicknesses are in multiples of .015 inches. The number of planes or the thickness of planes is not a limiting factor.

2. Depending upon end use of the composite, the metallizing composition is a refractory metal such as tungsten or molybdeum, or a noble metal such as palladium, platinum, or other suitable alloys. The noble metals can be specified when the composite is to be used in applications requiring air-fireable thick film materials. Metal thickness of .002 to .001 inch are normal with electrical resistances as

low as .007 ohm per square obtainable. Both refractory metal and noble metal composites are available from ceramic manufacturers. Conductor widths of .010 inch or greater with .010 inch or more space between lines are recommended where possible. Maximum economy is achieved with line widths of about .015 inch and .015 inch or greater spacing, with greater spacing more desirable than wider lines when trade-offs must be considered. However, .004 inch lines and .008 inch centers can be provided.

In some instances even finer patterns are possible, but these must be considered on an individual basis. Cost increases as line widths and spacings decrease especially when long parallel paths are encountered. Conductive line width tolerances of plus or minus .002 inches are practical with plus or minus .0005 inches possible in optimum cases. Tight tolerances increase inspection and manufacturing costs and should be specified only when needed.

3. The use of vias, or conductive risers, is the most popular method of interconnecting the metal planes; in other cases, metal over the edges of the substrate may be used. A minimum via diameter of .005 inch with minimum centerline spacing of .010 inch is possible with .002 inch thick insulating planes. Thicker insulating layers require larger vias with spacings between adjacent holes no less than the thickness of the insulating layer. A minimum centerline spacing of .025 inches for vias is recommended. Vias of .015 inch in diameter or less are preferred, but when possible exact size should be left to the discretion of the supplier.

   In most cases, it is desirable to cover each via hole with a metal "cover dot." These cover dots allow for slight manufacturing misalignment and must be considered in the spacing of adjacent lines. The cover dot may be as small as .015 inches diameter but should be .020 inches in diameter when space allows. When through risers must be hermetic, it may be necessary to break the riser with a short internal offset.

4. Buried conductors directly under chip bonding areas requiring flatness or coplanarity should be avoided when possible.

5. The buried conductors are, of course, unplated. All exposed refractory metallized areas normally receive nickel and gold plating. Designs requiring fine, isolated pads and imbalance of plating area will create plating problems. While these should be avoided when possible, they sometimes can be handled with modern plating techniques. Noble metal patterns may not require plating.

6. External electrical contact methods include ribbon leads, pins, or contact edges for plug-in board type of connections. Parts can be supplied with or without pins or leads. The use of pins will increase tooling and assembly costs and should be avoided when economy is a consideration. Since hermetically sealed conductors can be brought from the device area to the external contact area, the necessity of hermetic sealing of pins is eliminated.

7. Several approaches may be taken to the problem of providing hermetic protection for the chip area. The most often considered are:
   A. Cup-shaped lid: A metallized band on the top surface provides a seal area for a matching cup-shaped lid.
   B. Recessed cavity: Recessed area which will accommodate chips may be included in the design. A seal ring on the top plane then allows a flat cover to seal off the chip-containing area.

8. A standardized system is used between the supplier and the user to designate the various planes. One common system is to have all ceramic planes carry a CP prefix plus a number to designate the plane's location in the composite.

All metal planes carry a MP prefix. Thus the bottom or base ceramic becomes CP1; the metal pattern applied to the top CP1 is MP1; the next insulating layer is CP2, etc. If patterns are required on the back side of the base, the bottom surface of the base becomes CP01, and the metallized plane on the bottom is MP01.

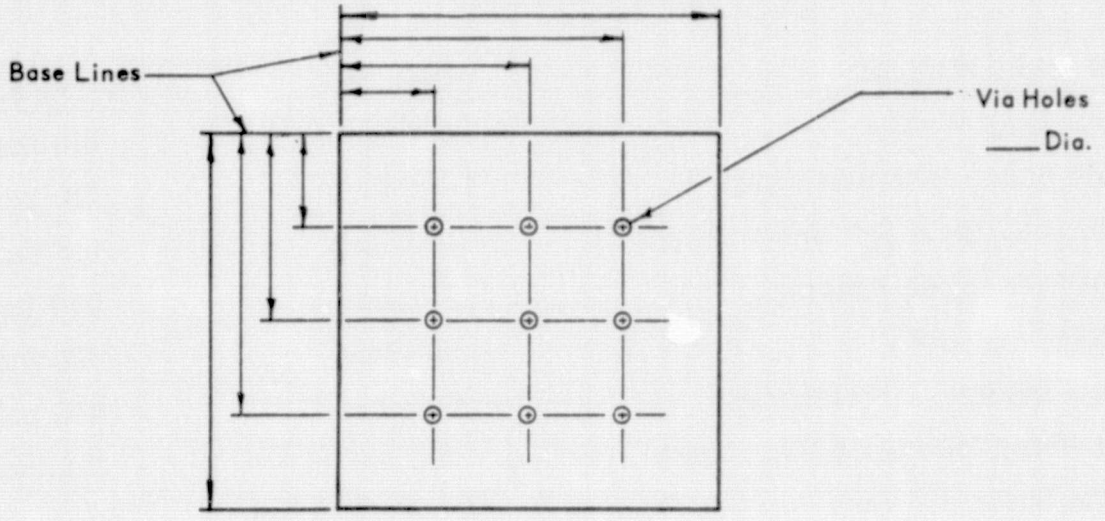
9. Detailed drawings and specifications must be supplied to the composite or multilayer manufacturing. These drawings should be 10:1 or larger, and there should be one drawing for each metallized plane and one for each ceramic plane showing via holes. Who should supply the necessary artwork is a matter to be resolved between the user and the supplier for each case in question.

Before a circuit designer gets too far along on his design, using ceramic composite wiring structure, he should contact the supplier to determine the exact design parameters that apply to his particular case.

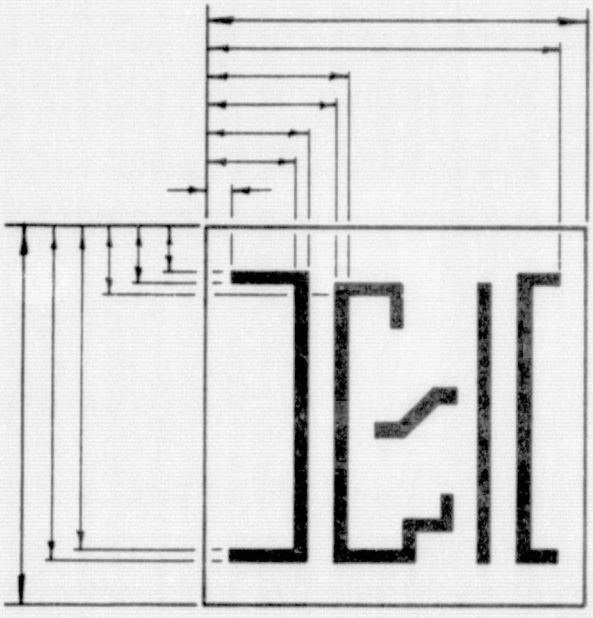
DESIGN PARAMETERS	POSSIBLE	PREFERRED
Minimum Line Widths	.004 inch	.010 inch
Minimum Space Between Lines	.004 inch	.010 inch
Via Hole Dia. (best left unspecified)	.005 inch	.015 inch
Via Hole Centerline Spacing	.010 inch	.030 inch
Via Hole Cover Dot	.015 inch	.020 inch
Via Plane Insulation Thickness	.002 inch	.005 inch
Non-via Plane Insulating Thickness	.002 inch	.015 inch multiples
Maximum Substrate Size	6 inch X 6 inch	3 inch X 3 inch

TOLERANCES		
Line Width	± .0005 inch	± .002 inch
Conductor Centerline Spacing	± 1/2% NLT ± .002 inch	± 1% NLT ± .005 inch
Substrate Length & Width	± 1/2% NLT ± .002 inch	± 1% NLT ± .010 inch
Substrate Thickness	± 10% NLT ± .002 inch	± 10% NLT ± .005 inch
Camber	.001 inch /inch (ground)	.006 inch/inch NLT .002 inch
Thru Hole Diameter	± 1/2% NLT ± .002 inch	± 1% NLT ± .005 inch
Pattern to Thru Hole or Substrate Edge	± 1/2% NLT ± .005 inch	± 1% NLT ± .010 inch
Metallized Pattern Resistance	.007 ohm/sq.	.015 ohm/sq.

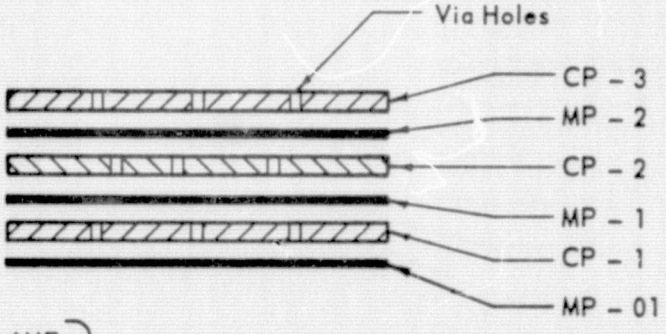
2.3.6.5.2 Preferred Method for Dimensioning Alsibase Composite Substrates



CP 1



MP 1



CP = CERAMIC PLANE
MP = METAL PLANE

SHOW DETAIL OF EACH PLANE

NOTE:
(1) USE BASE LINE DIMENSIONING OR GRAPH PAPER WITH EACH SQUARE = .005 inch
(2) SPECIFY DEGREE OF ANGLE WHEN CRITICAL

2.4 Computer Aided Design

The need for miniaturized devices and systems has been a primary factor in encouraging development of hybrid circuitry. The manifold increase in packing density makes the search for an efficient layout and interconnect pattern a difficult and time consuming task for skilled personnel. In addition to the layout and interconnect task, manufacturing requirements of high precision boards may often require the artwork accuracy which only automated drafting machines can deliver. Therefore, a cost effective computer aided design system for layout and artwork could be desirable in many instances.

Of the computer aided design systems used in the electronic industry, the interactive graphic design approach is particularly suitable for multilayer hybrid design. The problem of multilayer board design is a conceptual one, a problem of pattern recognition and intuitive judgment. In dealing with a task of this type, no system approaches the effectiveness of the experienced designer in determining an effective solution. An interactive computer aided design system implements the computer for its characteristic speed and accuracy while retaining the human element to provide creative judgment. Before a discussion of multilayer board design application proceeds, familiarity with some of the difficulties encountered in solving conceptual problems as opposed to other types is desirable.

2.4.1 The Nature of the Problem

Computers perform many functions in modern technology, business and industry. The computer is programmed to execute innumerable tasks ranging from circuit analysis in airborne navigation systems to printing utility bills. All of these tasks though they may seem dissimilar, can be grouped under two job classifications, manipulative and deterministic. The differentiating criteria for classifying these various tasks is found in their methods of solution.

First, consider the manipulative task. Under this classification are tasks such as accounting as applied to most commercial and municipal jobs. Routines consist mainly of data manipulation through sorting, merging and updating

data files. Mathematical operations are generally simple and repetitive. The generation of report listings is often a large part of this data processing operation. Although the typical programming is complex, programs can always be written which will yield a definite answer.

The second job classification is that which is deterministic in nature. For example, a program which calculates the circuit element values in a two-part RF filter is a deterministic program. Statistical calculations and navigational problems are also of the deterministic type. Mathematical operations tend to be complex and iterative. However diversified the task may be, there is one property common to all deterministic programming. A solution will be readied through a definable process and the method and output result can be predicted given a set of input conditions.

For both manipulative and deterministic problems algorithms can be devised which will unequivocably lead to a definite solution. However, another type of problem exists that does not fall into either of these two categories. This type of problem is that of a conceptual or judgmental nature. This problem has no straight-forward solution. Conceptual difficulties arise which require judgmental decisions contingent upon innumerable conditions. Routes to a solution are either so ill defined or relate to such a large number of combinations that no reliable strategy exists that will lead unfailingly to a solution. It is in these situations where heuristic techniques must be employed. Heuristic implies an empirical technique effective in yielding a solution but unproved; a "rule of thumb" if you will.

For example, a commuter uses heuristic techniques when driving his automobile across town. His good judgment, skill and experience guide him from point A to point B. Although a timely arrival is usually achieved, there is no guarantee that his heuristic techniques will adequately handle every variable encountered on his next trip. The computer is inefficient in solving conceptual and judgmental problems because effective heuristic algorithims are rarely definable. Again considering our orology, a commuter drives his car across town in nearly a subconscious mode of thinking making many decisions every

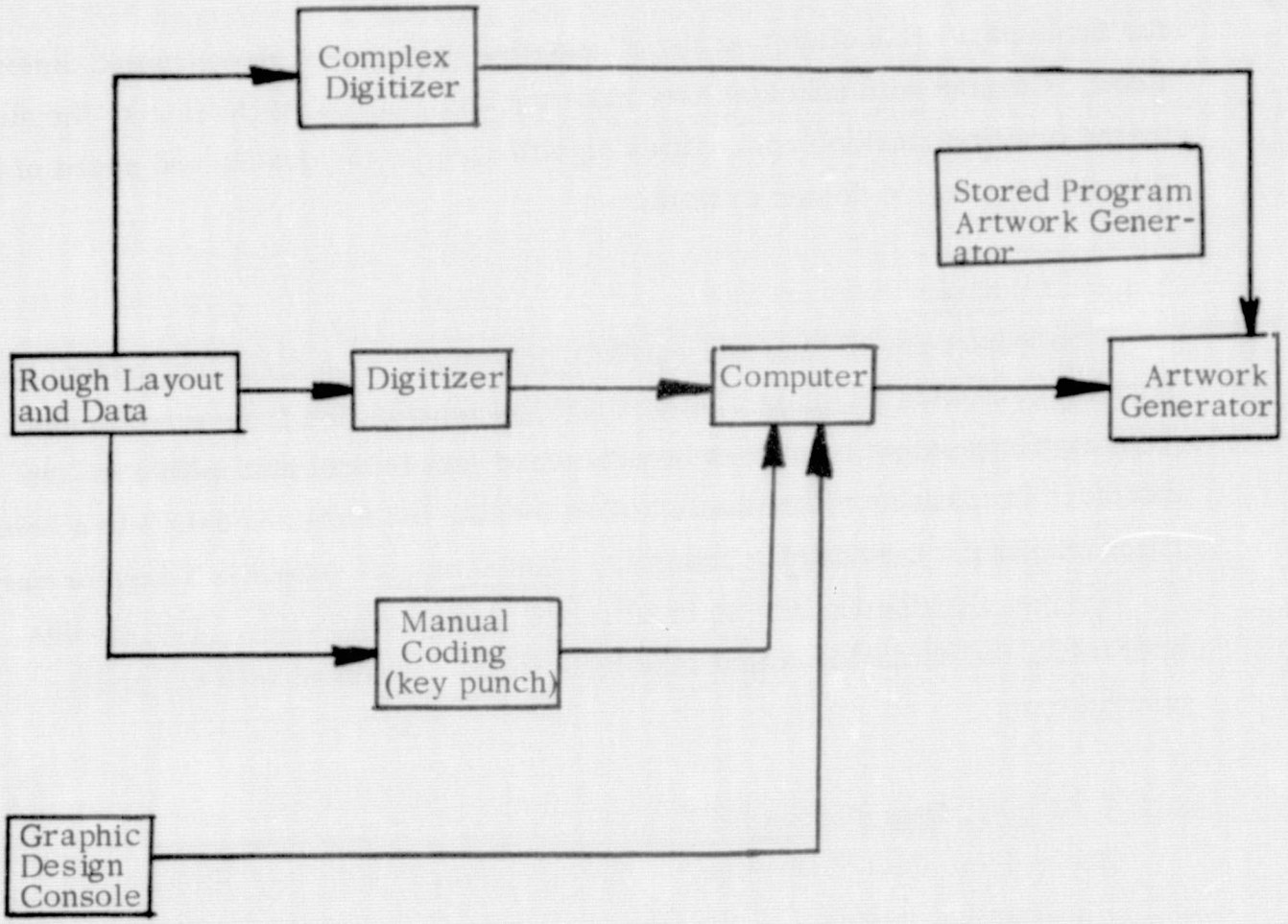
minute. However to write down the exact criteria for the judgment exercised in a cross-town trip is an impossible task. It is in this group of conceptual problems which we find the task of multilayer board design.

Heuristic techniques must be employed in order to determine a solution for a multilayer interconnect. However, there are no effective computerized heuristic algorithms which are capable of designing a multilayer interconnect without designer interaction. There does exist, however, program suites which are capable of designing layout and interconnect patterns of double sided circuit boards using heuristic routing algorithms alone. The success of these programs can be directly attributed to several foregoing assumptions which are integral to the routing algorithms employed. The principal assumptions are: (1) vertical and horizontal routing will be done on opposite sides of the circuit board; (2) two and only two layers will be designed; (3) few or no discrete components will be used; (4) all device geometry will conform to a standard grid. More of these assumptions can be made in regard to multilayer board design. Even in the most advanced program suites of the non-interactive type manual intervention and multiple iterations are often required. The computer alone cannot be programmed effectively to solve conceptual or judgmental problems but the experienced designer does have this ability. The most effective system then, would be one in which a designer asserts his judgment in solving the conceptual aspects of the multilayer design problem. The computer would then be used to assist the designer by doing the "busy work" of drafting, data storage and artwork generation. This, in essence, is the interactive graphic design concept.

The interactive graphic design concept is quite applicable to layout of complex multilayer circuits. However, the amount of data storage required to develop a complete computer layout of a complex circuit would exceed the capabilities of most circuit fabrication facilities presently in operation.

It is felt that computer use in layout will continue to grow with the requirements for more complex multilayer circuitry. Facilities that do not have computer aided design capabilities will either become dependent upon layout

establishments possessing computer aided design equipment or convert their own design and layout procedures to that of computer and automated artwork generation.



2.4.2 Artwork Generators

The artwork generator is not merely a machine, but a precision tool manufactured by precision tool makers. Considering all the devices which comprise an interactive graphic design system, the artwork generator is the most significant factor in determining accuracy, repeatability and the rate of artwork production. A quality plotter can be expected to produce precise lines with sharp edge definition without swelling, necking or wiggle. Although accuracy will vary between plotters one can expect a positional tolerance of .001 inches with a repeatability of .0005 inches or less. In commenting on speed, it is sufficient to state that overall plotting time is a small fraction of the time required for manual drafting. Precision artwork generators yield still another feature in addition to simply producing quality artwork. Precise artwork can be produced in smaller scaled dimensions thus reducing the need

for large photo reduction thereby eliminating subsequent photographid distortions. Coupled with efficient data inputting and control mechanisms, the automated drafting machine contributes significantly to the quality and speed of the interactive graphic design system.

2.4.3 Digitizer

The generation of tape and cards is performed by a digitizer, coding the layout coordinates together with line and pad information from a rough sketch. This digitized output must then be processed into a form compatible to the plotter. Processing is accomplished by feeding the digitized data into a computer containing a modifying program. The computer output is a tape or card deck now acceptable for use as input to the plotter controller. For on-line operation, the computer output may be directly interfaced with the plotter control unit.

2.4.4 Graphic Design Console

The graphic design terminal is the input-output point for the human element in the interactive system. Both circuit layout and digitizing may be accomplished by the use of the graphic deisgn console. Consisting of a CRT (Cathode Ray Tube) display and a means of layout generation, either by light pen or stylus drawing tablet, the console is used in conjunction with a computer to modify the console output into a format suitable for the plotter. Components may be called up from a storage library, interconnections sketched, and then the CRT display pattern can be visably checked for accuracy before artwork generation.

2.4.5 Complex Digitizers

Complex digitizers are available from some suppliers to complement their particular plotting table. The output information from these special digitizers is automatically processed and in a form directly acceptable to the plotter without the need of further computer processing. Complex digitizers can be used on line with a plotter to provide simultaneous artwork generation.

2.4.6 Inputting

Data transmitted to the artwork generator requires some input processing in order to achieve interface compatibility. For off-line interfacing, the input data which consists of digitized layout coordinates and line and pad information is stored on magnetic tape, paper tape or cards. The intermediate processing step between the digitizer and plotter is actually done by a computer containing the modifying program. The resulting batch data, now compatible with the plotter, is also stored via a peripheral medium such as tape or card. At the desired time this compatible data is fed to the plotter for artwork generation.

For on-line operation, the computer output may be hard wire interfaced with the plotter control unit. However, this method may not be practiced because this places the computer in a peripheral stand-by condition.

2.4.7 Plotting Check

Plotting check capability usually is a part of such an interactive system. Errors or violations are shown on a pen plot generated by a plotter interfaced with the computer. Generally, changes to the design layout can easily be made at this stage of processing by a simple change to the computer submitter through the CRT design console. Only a few iterations are normally required to obtain a final correct layout on most systems.

2.5 Artwork Generation

Artwork generation can be considered that area of endeavor between the circuit substrate layout and the delivery of the screen fabrication films. The completed engineering layout is used as a basis for generation of both the multiple scale master patterns and the assembly drawings. It may be found that the initial layout scale is not large enough to give the accurcay required for close tolerance, high density multilayer circuits. If a higher scale is required, an accurate blown up layout can be drawn and used both for the final assembly drawing and the basis for dimensioning the master pattern.

The final assembly drawing procedure depends upon the drafting format used at the engineering organization responsible for the documentation effort.

2.5.1 Final Assembly Documentation

The final assembly documentation should include the following:

1. Final assembly envelope drawing.
2. Final substrate assembly.
3. Master pattern artwork.

2.5.1.1 Final Assembly Envelope Drawing

This drawing should show the final circuit in its completed stage. The drawing should contain the physical dimensions and its electrical specifications. Any sealing and leak testing specifications should be shown as well as any environmental testing specifications which apply.

2.5.1.2 Final Substrate Assembly Drawing

This drawing is the final version of the layout drawing and should show a complete parts list with applicable material nomenclature. A schematic of the total circuit should be shown with appropriate reference designations, values, and tolerances. Any assembly and fabrication specifications which apply should be shown.

2.5.1.3 Master Pattern Artwork

The master pattern artwork may be of the cut rubylith type or the older system of taping. The rubylith masking film consists of a transparent sheet of polyester backing film to which a thin layer of red transparent plastic has been laminated. The thin layer of red material can be cut very easily and lifted or peeled from the backing sheet. This type of film will photograph black in the red areas and white in the clear areas. Negative printing can result from the operation of peeling either background or pattern.

The older system of taping consists of using black or red adhesive coated polyvinyl tape which is commercially available in precision widths. The tape is applied opposite to cut and peel as the image is added rather than left by removal of excess material.

To make either type of master pattern, the drawing or sketch of the circuit (blown up by the desired amount) is placed beneath the transparent film (mylar for taping or rubylith for cut and peel). The tape is applied and fitted to the circuit configuration by cutting to length. Various widths of tape are available to build up to desired geometries. The mylar is cut along the outlines of the image required and the excess is removed. Excellent accuracy can be obtained in either method but where extreme accuracy is required, a coordinatograph should be used.

The coordinatograph offers a more accurate method of master artwork preparation as well as eliminating the requirement for an accurate layout. A knife for cutting the rubylith is mounted on the movable carriage of the coordinatograph and performs the cutting operation as the carriage is moved in the X and Y direction. Holes and circles can be cut with sufficient practice using some of the available equipment.

2.5.1.3.1 Alignment and Registration Marks

A set of registration marks must be provided on each film layer to facilitate alignment between films and as a tool mark for screen registration between layers.

FIGURE 2.5-1
TYPICAL REGISTRATION MARKS

2.5.2 Reduced Film Master

The completed master pattern artwork is processed in an appropriate photo reduction laboratory to achieve an accurate 1:1 film master positive with the emulsion on the screen contact side.

2.6 Thick Film Substrate Fabrication

Thick film substrate fabrication is not as critically dependent upon clean room conditions as that of thin film and monolithic circuit fabrication. Clean room conditions are maintained; however, to satisfy exacting requirements. The most critical functions dependent upon clean room conditions are screen fabrication and actual screen printing prior to firing operations.

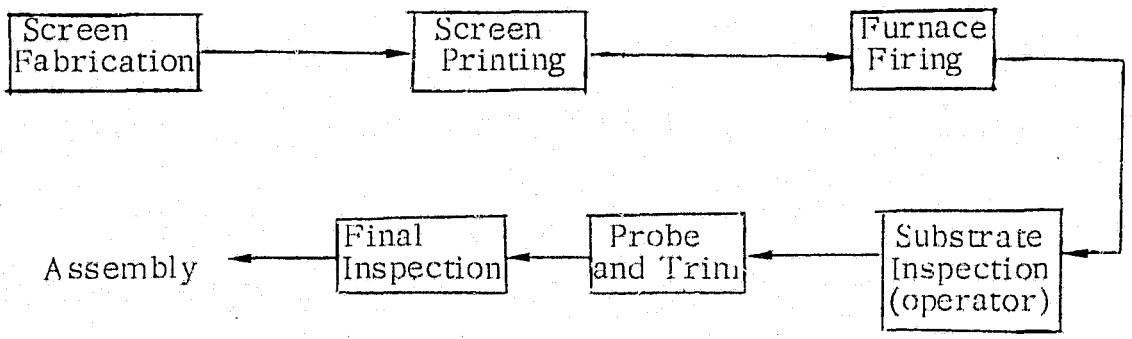


FIGURE 2.6-1
SUBSTRATE FABRICATION FLOW CHART

2.6.1 Screen Fabrication

It should be readily apparent that definition and repeatability of processes are critically dependent on the integrity of the fabrication screens. It would be less than satisfactory to attempt to control materials and workmanship without incorporating controls on screen fabrication. Some establishments purchase screens made to their specifications and/or artwork. At times, subcontracting the screen fabrication may result in long delivery delays and unsatisfactory results. It has been found that it is more economical both in time and cost to become proficient in screen fabrication thereby maintaining close in-house control of this very important tool.

The mesh size used depends on the application: 160 to 200 mesh is commonly used for resistors and dielectrics 200 mesh is used for conductors over .008 inch in line width. Fine line conductors, less than .008 inch in line width, usually require 325 mesh screens.

The screen tension is a critical element in screen fabrication as it determines the speed of "snap off" and the distance from the screen to substrate or "break-away," as this distance is frequently called. Too little tension results in distortion in printing caused by excess distance the screen is required to be deflected to obtain a good print.

2.6.2 Types of Screens

There are three basic types of screens used in thick film fabrication (a) etched metal mask, (b) direct emulsion, and (c) indirect emulsion screens.

2.6.2.1 Etched Metal Masks

The etched metal masks have been found to allow the best definition in printing both contact and off-contact applications. However, the rigidity of the metal masks prevent conformity to the uneven topography encountered in multilayer substrate fabrication. The expense of etched metal masks is also considerably higher when compared to the flexible screens of either direct or indirect emulsion types.

2.6.2.2 Direct Emulsion Type Screens

The direct emulsion type screen is fabricated by first stretching the screen material (see Materials section 2.7) over a suitable frame and bonding or attaching it to the screen printer frame. Studies have shown that the best definition of lines is obtained when the screen is mounted with the strands of the screen material placed on a 45^{O} angle to the circuit X and Y axis. The frame and screen are then cleaned to remove any foreign material which could effect the image development. After cleaning, the screens are ready for application of emulsion. Many types of direct emulsion materials are available and several methods of application are known such as flow coating, spray, brush and squeegee application.

The following is a description of a common procedure for fabrication of direct emulsion type screens. Screens are selected of the mesh and material appropriate to the required circuit line width, thickness and spacing. The screen is trimmed and installed on a stretcher frame for stretching, with screen strands positioned parallel to the stretcher straight edges. The stretcher frame is expanded to achieve proper screen tension. Printing frames are oriented to present as nearly as possible a 45 degree difference between the screen mesh axes and the

printing frame sides. The stretcher frame is lowered so that the stretched screen engages adhesive coated surfaces of the printing frame, and remains engaged for the adhesive cure time specified. After the adhesive has cured, the screen is neatly trimmed around the outer edge of the adhesive bond area. The screen and frame are then cleaned just prior to application of emulsion.

The prepared precast print frame is set up with the screen side down against the clean glossy surface of a sheet of acetate, positioned on the top surface of a plexiglass plate. The plexiglass plate is sized to fit inside the screen frame so as to clear adhesive bonded areas. The glossy surface of the plastic sheet is free of scratches or other surface irregularities. This operation should take place in a laminar flow bench.

A small quantity of the prepared emulsion is squeeged onto the screen surface. Fifteen minutes minimum drying time is allowed at room ambient and then a second coat of emulsion is applied. The second coat is allowed to dry for 30 minutes minimum. Coated screens are exposed and developed within 16 hours after being coated. The acetate sheet is not removed until immediately prior to the printing exposure operation. All processes involving photo-sensitive materials are performed under photographic "safe" light conditions.

The finished screens must be capable of producing screened circuits of clean definition, and must be free of pinholes, flakes, and other contamination or surface irregularities as observed under 30X magnification.

2.6.2.3 Indirect Emulsion Type Screens

The indirect emulsion type screen is fabricated much like the direct type with the exception that the image is developed prior to emulsion application to the screen. The indirect emulsion is a light sensitive material mounted on a sheet of backing material. The image is developed by placing film master in contact with the light sensitive film and exposing it by the manufacturers

prescribed method. The exposed image is then developed to obtain the desired image while the material is still attached to the backing sheet. The developed image is then attached to the screen with a squeege and allowed to dry. After drying (cure), the backing sheet is peeled off leaving the image attached to the screen. The indirect emulsion type screens have been found not to be as durable as the direct type emulsion in extended use.

2.6.3 Screen Printing Equipment

Most screen printers used in multilayer substrate fabrication are of the hand operated type or the semiautomatic type. In the hand type operation, the screen is mounted in a frame which also holds the substrate in relation to the screen during the printing operation. The thick film paste is placed on the screen and forced through the screen with a hand-held squeege. The hand printer is useful for small quantity work and for non-critical applications; however, the parameters necessary for precision results are extremely difficult to control in a hand printer.

The commercially available semi-automatic printers are accurate precision instruments which can be set up and large quantities of substrates processed with little change in results expected. Most modern screen printers have adjustments for X, Y, and circular positioning as well as break away or Z adjustments. Most printers also have vernier adjustments and/or micrometer readouts.

2.6.4 Substrate Processing

Many technical papers are available which deal with the processing of screen printing, probably the best publication for reference is the DuPont Thick Film Handbook which is available from the company. The following is a generalized description of substrate processing sequences.

2.6.4.1 Thick Film Application Process

The substrates to be processed are cleaned in liquid detergent and tap water. They are then rinsed in flowing non-recirculated water and blown dry with a jet of nitrogen, at not more than 50 PSIG, directed across the surface

of substrate. Cleaned substrates are stored in appropriate enclosed containers that are non-deleterious to subsequent processing. Containers are cleaned prior to use.

Appropriate printing frames are installed in the holder and aligned to achieve proper screen registration with the substrate. The vertical spacing between the screen and the substrate is adjusted for precise parallel alignment. The spacing between screen and substrate is adjusted to approximately 0.025 inch for first trial run.

All paste materials are well stirred upon receipt with a stainless steel spatula. Stirred jars of paste are stored on a 45 degree active mixer that is rotating at one to three RPH. Paste from inactivated storage is thoroughly stirred until homogenous immediately prior to use. When preparing blends of pastes, to achieve intermediate resistance values for example, the following procedure is used.

1. Each jar of paste must be stirred thoroughly before the required amount of paste is removed.
2. When a small amount of one paste is to be blended with a larger amount of another paste, a comparable volume of the larger shall be added to the smaller one, and then stirred for a minimum of five minutes.
3. Subsequently, the remaining amount of material is added in small increments and stirred to uniformity after each addition until the blending has been completed.

When intermediate resistor values are to be obtained it is desirable to blend adjacent resistance value compositions in the series rather than those which are separated over a wide range.

The paste of the highest firing temperature is selected for the first screening application. The printer is cycled to produce a sample deposition of material and adjusted as required until proper screening is accomplished. An adequate

supply of paste is maintained on the screen to ensure complete screening of circuits. All substrates after printing are dried under radiant heat at 125 degrees ± 15 degrees Centigrade for 15 minutes minimum prior to firing, depending upon the characteristics of the paste material applied.

Substrates are placed on the conveyor belt of a continuous belt furnace for the appropriate firing cycle. Optimum belt speed and temperature curve profiles are in accordance with established optimum criteria for the various paste materials to be processed. Precise firing cycle data are recorded for each production run of deliverable substrates. Established temperature profiles are maintained within ± 5 degrees centigrade. The rates of temperature rise and temperature fall ahead of, and following, firing level are within 30 to 70 degrees centigrade per minute. It is desirable for a given profile, that control be held to within ± 5 degrees centigrade per minute along with the rising segment of the profile.

2.6.4.2 Visual Inspection

The operator performing the screening operation should perform systematic inspection of the substrates being processed. This not only allows the operator to be aware of processing problems but also allows the operator to make mechanical adjustments at a time before a large quantity of substrates have been processed. The substrates should be inspected at each level of screen printing prior to substrate firing as repairs to damaged conductor and dielectrics are more readily performed in the unfired state.

Processed thick film having thin or open areas, damaged sections, or excessive material may be reworked as follows:

Thin or open areas and damaged sections may be reworked by adding the appropriate paste material. Paste is applied over a thin area, unbridged area or damaged section and fired at the last firing temperature. In cases of excess material, the excess may be removed by scribing with a diamond scribe or air abrasive. Care is taken to prevent damage to the substrate.

Quality adhesion test samples should be made weekly. These adhesion monitor patterns are submitted to Quality Control for pull testing as initial material evaluation. Each substrate is examined after firing, using a minimum of 30X magnification and back lighting. This serves to verify the integrity of the screen as well as the printing process.

2.6.4.3 Probing

The conductors should be optically inspected as well as electrically probed at each level for opens and shorts. Repairs to buried layers are difficult or impossible to perform be they opens or shorts, making prevention of such problems manditory.

Electrical testing of a complex ceramic multilayer circuit can consume a significant amount of time and labor. Continuity checks between conductor layers after each firing can bolster confidence, but the entire circuit must be tested before devices are attached. Care must be taken to design the test apparatus so that high resistance shorts between layers can be detected. If the fabrication quantity is sufficient, automated testing is warranted. Testing of small quantities by the point-to-point continuity check method is tedious and requires a complete set of conductor artwork at the test station.

2.6.4.4 Trimming Thick-Film Resistors

Prior to trimming, the resistor will have been established as being within the required trim range. The substrate is placed on a platform in the trim station so that the resistor is centered beneath the abrasive nozzle or a laser beam. The resistance bridge monitor probes are lowered to make contact with the resistor terminals. The bridge is adjusted to the required resistance, and the trim speed control adjusted for the desired feed. When the programmed resistance value is obtained, the bridge will cut off abrasive flow or laser beam automatically.

In cases where resistors have been trimmed beyond usable tolerance, or damaged beyond acceptable limits, circuitry may be repaired as follows:

A resistor may be scribed open at both ends using established techniques and a chip resistor installed in its place. Installation of chip resistors will be in accordance with the established procedures for electrical and mechanical bonding of components. The replacement chip resistor must be capable of meeting all physical and electrical characteristics of the resistor that it replaces.

2.6.4.5 Sizing

Unless otherwise specified, sizing of thick film substrates should be performed before resistors have been trimmed. The sizing tool is usually a sharp tip diamond scribe which is positioned in the sizing fixture approximately 10 degrees from the vertical, with the slope in the direction of scribe movement.

With the substrate held firmly in position, the scribe carriage is pushed across the substrate surface. The substrate is broken apart on the scribed line. Some facilities use a laser beam instead of a diamond scribe for sizing.

2.7 Materials

A list of materials associated with the fabrication of multilayer ceramic circuits would be of considerable length. Each area of endeavor has its own particular materials usage. In this section, the materials will be discussed in relation to their specific application in tooling and circuit fabrication. The following grouping of subject materials will be discussed.

1. Solvents and cleaners.
2. Screen associated material.
3. Substrates.
4. Thick film pastes.
5. Assembly materials.

2.7.1 Solvents and Cleaners

Most hybrid facilities have a series of proprietary cleaning procedures for the various fabrication and assembly operations with which they are involved. As in the case of substrate cleaning, these processes ususally involve multiple steps of detergent cleaning, deionized water rinse and alcohol or other solvent rinse.

The detergents used should be analyzed to assure the user that no residues will be left on the part being cleaned. "Sparkleen" detergent seems to meet most of the requirements of a non-residue cleaner and is used extensively in fabrication of multilayer circuits. As with detergents, solvents should be analyzed to determine residue characteristics, cleaning ability and reaction with tooling materials such as screen emulsion and squeege blades. Substrates should be checked at all stages of fabrication to assure the absence of residues. Some of the adverse affects seen from these residues include blistering of conductors and dielectrics, pinholing in dielectrics, peeling and poor adhesion in conductors and poor repeatability in bonding parameters. It is also suspected that resistor repeatability may be adversly affected by contaminants left on the substrate.

2.7.2 Screen Associated Material

The materials commonly associated with screen fabrication include frames, screen material, adhesives and emulsions.

2.7.2.1 Frames

Screen frames are commercially available from the screen printer manufacturer as well as various screen fabrication houses and screen material suppliers. The frame used should be structurally stable and designed to fit the particular printer being used. Some screen printer manufacturers offer adapter mechanisms to allow the use of different size and design of screen frames other than the ones specifically designed for their printer. The most economical approach is to use a screen frame that can be reclaimed for reuse after the existing screen is outdated or damaged.

2.7.2.2 Screen Material

The screen materials currently available are of two types, metal cloth and plastic cloth. Various types of weaves are available including twill and plain weave. For most purposes, the plain weave wire cloth in stainless steel appears to be best suited to multilayer ceramic circuit fabrication. There exists considerable argument concerning plastic screen versus steel wire screen for multilayer work. Plastic cloth such as nylon, does seem to conform to uneven topography as well or better than steel mesh but the distortion resulting from the stretching characteristics during printing seems to be significant. The cost of the plastic screen material is less than that of the steel which may be a factor in the wide spread use of plastic screens in Europe. The screen mesh size used in multilayer substrate fabrication varies from 160 mesh to 325 mesh depending on application (see Screen Fabrication section 2.6.1).

2.7.2.3 Adhesives

The adhesives used in attachment of the screen material to the screen frame should have a fairly rapid cure time and good structural integrity after curing. The flow characteristics should be good with low viscosity to allow penetration through the finer mesh screens during bonding. The adhesives should be impervious to moisture and solvents and not be adversely affected by use and storage.

2.7.2.4 Emulsions

The photo sensitive emulsions used in multilayer application are of the two types, direct and indirect emulsion types as discussed in the Screen Fabrication Section 2.6. The emulsion system should be closely checked to determine the definition characteristics, wear, solvent resistance, and structural integrity. An evaluation should be performed with the emulsion to be used to determine its applicability to the processes to be used in circuit fabrication. The test patterns recommended in the Test Pattern Utilization section, 2.8, can be used for evaluation of both materials and processes. Any minor defects in screens can be touched up using water soluble block-out solution. Block-out solution can also be used where resistors of different sheet resistivities are placed on one screen. The desired resistor can be printed while the remainder are blocked out. The water soluble block-out solution can be removed by exposure to running water and blowing dry. The previously printed resistor can then be blocked out and the next desired sheet resistance printed.

2.7.3 Substrates

The choice of base substrate material is one of the most important decisions to be made in multilayer ceramic circuit design. The substrate is the very basic foundation upon which the multilayer is fabricated, assembled and tested.

Many factors must be considered when choosing the materials to be used for substrates. Among these are fabrication techniques, packaging philosophy, mechanical and thermal parameters, electrical characteristics and end item usage. Obviously, the primary function of the substrate is to provide a mounting area for components while providing intercomponent isolation. The substrate is also expected, in the case of multilayer circuitry, to provide a plane for developing interconnect conductor systems between components and to external connections.

In selecting a substrate material, it is important to investigate its strength, thermal properties, application to design, and cost. It cannot be assumed that

the substrate is an inert object with no effect on the electrical performance of a completed circuit. Some of the most commonly used substrate materials are listed in Figure 2.3-5 with some of their most important circuit related characteristics tabulated.

Glass substrate and glazes have advantages in high frequency applications, but the lower required firing temperature makes them unusable with most commercially available conductor/dielectric systems. Many of the paste manufacturers are currently developing low firing conductor/dielectric materials for liquid crystal display systems that may prove applicable to multilayer circuitry on glass.

The most common base substrate materials are alumina and beryllia. Alumina in the "as fired" condition appears to be preferred for normal circuit application. Most commercially available conductor/dielectric materials are formulated to match the expansion coefficient of alumina causing a mechanical mismatch when fired on beryllia. The reduced adhesion and possibility of open or shorts must be considered when attempting to use the latter. Beryllia's exceptional thermal conductivity makes it very desirable for use in high power applications; however, caution must be exercised when handling, as the material is quite toxic when ingested. For most applications at frequencies to approximately 250 MHz and at moderate power levels, alumina substrates are quite adequate. At frequencies above 250 MHz where dielectric coupling becomes a more significant problem and/or at high power levels, the expense and handling problems in using beryllia may be worthwhile.

Ceramic substrates are available in a broad range of sizes and thickness and can also be obtained with arrays of holes or grooves. It is good practice to fabricate the thick film multilayer on the smallest substrate consistent with good layout and design practices. The substrate surface finish is related to adhesion of the cermet paste; generally a surface finish of 25 microinches or rougher is normal for good adhesion. Substrate flatness is also considered extremely important as warped substrates can set up stress/strain situations as well as cause considerably difficulty in printing fine line conductors. The normal specification is for substrates to have warpage less than .004 inch per inch.

MATERIAL	TENSILE STRENGTH (PSI)	THERMAL CONDUCTOR BTU/hr/ft/^{o}F	THERMAL COEF. OF EXPAN. 10^{-6} in/in/^{o}C	MAXIMUM FIRING TEMP. (^{o}C)	DIELECTRIC CONSTANT AT 1 MHz (25^{o}C)	RESISTIVITY AT 25^{o}C OHM - CM.
96% Al_2O_3	25, 000	10.0	8.0	1550	8.2 - 11.2	10^{16}
Glazed 96% Al_2O_3	25, 000	8.0	8.0	700	8.9	10^{16}
Steatite	10, 000	2.0	7.8 - 10.4	1000	5.9 - 6.1	10^{17}
Glass (General)	4, 000	0.4 - 0.8	0.8 - 1.3	600	3.8 - 15.0	10^{12}
Forsterite	10, 000	0.9 - 2.4	10.6	1000	5.8 - 6.7	10^{17}
Beryllia	14, 000	30.0 - 125.0	4.2 - 9.4	1500	5.8	10^{16}
Pyro Ceram	10, 000	1.1 - 2.1	0.2 - 4.0	700	5.5 - 6.3	10^{12}

FIGURE 2.3-51

2.7.4 Thick Film Pastes

The thick film pastes used in multilayer ceramic circuitry can be considered as being evolved from pastes used for years in standard thick film hybrid manufacture. The major break through in materials development came with the development of the crystallizable crossover dielectrics. Previous attempts at fabrication of multilayer ceramic circuits resulted in low yield due to the glass crossover dielectrics resoftening at each firing. The conductors in contact with the glass would sink through or "swim" in different directions resulting in a high incidence of shorts and opens.

The thick film pastes or "inks", as they are often referred to, can be grouped into these types: (1) resistor, (2) conductor, (3) dielectric and (4) special application materials.

Section number 3.2, Materials Evaluation Study, describes an in-house evaluation performed as a part of this contract to determine the characteristics of currently available conductor and dielectric compositions when applied to fine line multilayer ceramic circuit fabrication.

2.7.4.1 Resistor Pastes

There are a variety of resistor compositions available on the market at the present time. The demand for them has grown considerably in recent years making it practical and desirable for the paste producers to offer a wider range of characteristics and in some cases, lower costs as discussed in the Test Pattern Utilization section (2.8). The compatibility between resistor compositions and the conductor terminations should be suspect until sufficient in-house testing has been performed. Sheet resistivity of resistor pastes is specified in ohms/square by the vendor supplying the paste. This figure should be considered only as approximate since the processing conditions significantly affect the "as fired" resistance. A totally different set of values for a resistor can be achieved simply by terminating with a different conductor formulation. The parameters considered important in thick film resistors are given as follows:

2.7.4.1.1 TCR - Temperature coefficient of resistance is the change in resistance with a change in temperature in parts per million per degree centigrade (ppm/^{o}C. The following formula is used for calculation of TCR:

$$\frac{(\text{Resistance at } T_1 - \text{Resistance at } T_2) \times 10^6}{R_{T_1}(T_1 - T_2)} = \frac{\Delta R \times 10^6}{\Delta T(R)} = \text{TCR in ppm.}$$

Values are often given as "hot TCR" (+25^{o}C to +125^{o}C) and "cold TCR" (-55^{o}C to +25^{o}C).

2.5.4.1.2 TCR Tracking - The ability of different resistor compositions to match each other and maintain a constant ratio over a given temperature range.

2.7.4.1.3 VCR - Voltage coefficient of resistance is the change in resistance observed when various voltages are applied. This can be a significant factor when close tolerance resistors are checked on a relatively high voltage resistance meter.

2.7.4.1.4 Noise - The large quantity of particle interfaces in thick film resistors make them somewhat more subject to current flow fluctuations referred to as "noise". The noise measurement is quoted in decibles. The noise level of a resistor composition can become a critical factor in some high speed logic systems.

2.7.4.1.5 Stability - Stability or drift is the amount a resistor will change in value when subjected to certain environmental conditions such as high temperature, moisture or chemical attack. The stability of the resistor system can be a significant factor in high reliability long life time electronic systems.

2.7.4.2 Conductor Compositions

The conductor compositions must be the most versatile of the thick film element materials. The conductors must exhibit the ability to be easily applied

with good definition and integrity. It must serve not only as a signal carrier but also as a reliable bonding or terminating point for all electrical connections. It is important to evaluate the conductor system as to its inter-reaction with the materials with which it is to contact both during fabrication and during the assembly operations.

2.7.4.2.1 Metallization Compatibility

Different metallization materials are used for conductors and depend upon termination bonding requirements. High purity gold is used where minimum resistance, TC bonding and/or die brazing are required. Solder applications require the use of palladium gold or platinum gold alloys to prevent amalgamation and solder leaching during solder operations. On circuits where the low impedence characteristics of gold and the solderability of Pd Au or Pt Au is required, multiple screening techniques allow the operator to deposit any combination of materials simply by changing screen masks. Solder dams of dielectric are used to separate solder areas from the thick film gold interconnects to prevent solder migration into the gold rich areas.

In critical circuits, a dielectric sublayer is used under solder pads to improve adhesion. Laboratory tests have shown a remarkable improvement in post thermal shock adhesion through the use of this buffer layer.

The following table shows a comparison of metallization compositions and their uses. Silver bearing compositions are not recommended for high reliability programs.

CONDUCTOR COMPOSITION	DIE BOND.	WIRE BOND.	SOLDERING	RESISTOR TERM.	BURIED MULT.
Palladium/ Silver	No	Not recom.	Yes	Yes	Not recom.
Palladium/ Gold	No	Not recom.	Yes	Yes	Not recom.
Platinum/ Gold	No	Yes	Yes	Yes	Not recom.
Gold	Yes	Yes	Yes	Yes	Yes

C - 2

2.7.4.2.2 Line resistivity - The table below shows the approximate line resistivity of the various conductor compositions. This resistivity can be affected by line width and processing parameters.

CONDUCTOR COMPOSITION	RESISTIVITY OHMS/SQUARE
Palladium/Silver	.020 - .100
Palladium/Gold	.050 - .100
Platinum/Gold	.080 - .100
Gold	.003 - .010

2.7.4.3 Dielectric Compositions

The dielectric compositions used in multilayer circuit fabrication cannot only introduce shorts (pinholes) and opens (closed vias, etc.) but also adversely affect the conductors which are applied directly to them or come in contact with them. The interreaction between the conductors and dielectrics can have a significant effect on conductor resistivity, bondability and definition as well as cause opens and shorts. The dielectric leakage characteristics can also be affected by various conductor compositions.

A thick film dielectric material for multilayer circuitry fabrication should have the following characteristics:

Dielectric Constant (1 KC)	9 - 20
Capacitance	1200 - 1900 pf/in^2
Quality Factor (Q) 1 MHz	>500
Dissipation Factor	<1.5%
Insulation Resistance (ohms)	>10^{10} (100 VDC)
Break Down Voltage	>400 volts
Fired Thickness	1.8 - 2.1 mils
Via Resolution Capability	<12 mils

Most crossover dielectric manufacturers recommend double layers of dielectric either singularly fired or cofired. It has been found that occurrence of shorts has been reduced by screening and firing a single layer of dielectric followed by a second layer screened and fired.

2.7.4.4 Fritless (Glass-free) Conductors

There has recently appeared considerable literature concerning new generation conductor systems containing no or very small quantities of glass. The fritless conductor systems are available with silver, copper, aluminum, gold and nickel metals. The firing process produces what is known as a reactive bond mechanism to attach the conductors to the substrate. Compatability between the fritless conductors and dielectric systems currently in use is an unknown factor.

The Materials Study section (3.2) covers an evaluation of some of these fritless conductor systems.

2.7.4.5 Non-noble Metal Conductors

It appears that non-noble metal conductor systems are of considerable interest to hybrid manufacturers for advanced packaging applications and may lend themselves to MLB technology. The reasons for this interest are not completely obvious, but economics seems to be the most significant factor. Noble metal pastes of course, have increased markedly in price due to their high precious metal content. Other factors in favor of non-noble metal systems include resistance to solder leaching (thereby reducing losses), adhesion improvement, and obtaining copper or nickel systems directly without necessity of plating. The aluminum system could eliminate the need for vapor deposition to fabricate monometallic systems utilizing aluminum interconnects.

An attempt was made to contact other hybrid manufacturing laboratories to discuss their problems encountered in firing non-noble metal conductor systems. After contacting several users and paste manufacturers, the following important points were brought to light concerning some of the paste compositions.

1. Paste formulation is quite unique in the non-noble metal systems and requires processing which is not compatible with normal paste systems. The normal or average industrial paste composition contains organic solvents and vehicles which set or dry at approximately 100 - 125°C. These organic binders must be burned out during the firing or sintering operation in the furnace at high temperatures (usually 800° - 1000°C). This burn out phase requires an oxygen rich atmosphere to guarantee complete carbon consumption. Some of the non-noble metal systems nobaly those containing aluminum, copper and nickel can be quite sensitive to the presence of oxygen in the furnace during the firing operation and concentrations of over 20 ppm may result in catastrophic oxidation.

2. Compatibility between non-noble metal conductor compositions and dielectrics is an unknown factor as the currently available dielectric compositions require an oxygenating atmosphere for firing.

3. Most laboratories do not have available the sophisticated environmentally controlled furnaces required for firing non-noble metal systems.

2.7.4.6 Photo Printable Conductor and Dielectric Systems

The photo printable conductor and dielectric systems appear to result in extremely fine line definition. The conductor systems are capable of .002 inch lines with .003 inch spaces and the dielectric with .005 inch vias.

The conductor or dielectric material is applied in a continuous sheet over an entire substrate or in selected areas. After drying, the layer of green fixed paste is exposed to a light source similar to screen fabrication. The photo sensitive material is then developed using a solvent spray. After drying

the pattern is fired in a standard processing furnace to obtain the final configuration. These photo printable systems show exceptional promise in multilayer ceramic circuitry use.

2.7.4.7 Special Application Pastes

The special application pastes include the screen printable epoxies and solder and braze compositions. These materials are formulated in a normal manner with the exception of being in a finely milled state with adequate organics and solvents to allow them to be screen printed.

The epoxies are available both in conductive as well as non-conductive types and are used primarily as adhesives. The solder and braze compounds can be used for component termination, mounting and for sealing operations.

2.7.5 Assembly Materials

The area of assembly materials is such a broad subject that it will only be discussed briefly here. The materials used in assembly include cleaning solutions, adhesives, bonding wire and sealing materials. All materials used should be kept under strict quality control and a comprehensive evaluation should be performed before commitment to an assembly operation.

2.8 Test Pattern Utilization

One of the most important and useful tools in substrate interconnect design is the test pattern. A conductor, dielectric or resistor test pattern, if correctly designed, can serve many purposes. Using an appropriate test pattern, not only can the materials themselves be evaluated, but the processing equipment and the operators performance of the function may be conditioned for optimum results.

2.8.1 Test Pattern Design

2.8.1.1 Resistors:

Resistor materials may present a compatibility problem with the dielectric materials and/or conductors used in multilayer circuits. Whether resistors are printed on the bare substrate or on a dielectric layer, samples should be fabricated to determine the "as fired" electrical parameters achieved with the specific combination of materials to be used in the circuit. The most appropriate configuration for a resistor test pattern is the "one square" configuration as shown in Figure 2.8-1. A series of one square resistors are printed ranging in size from .020 inch square to .250 inch square. A .015 inch conductor overlap is used at each end of the resistors for termination.

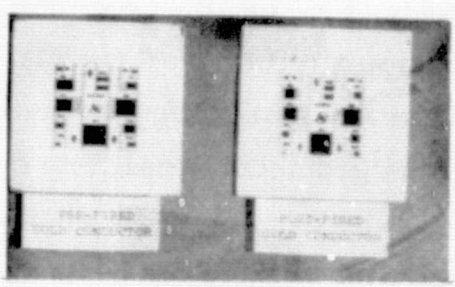


FIGURE 2.8-1. RESISTOR TEST PATTERN

It is advisable that a quantity (minimum of 10 samples) of substrates be fabricated using the specific combination of materials to be incorporated in the design. This sampling can be used to evaluate the exact reactions to be encountered during actual substrate fabrication. Some of the variables which could affect the "as fired" resistivity are as follows:

2.8.1.1.1 Resistors on Dielectric Layer - In some instances, resistor material will interract with the dielectric material to form an entirely different composition than expected. The resistor may become unstable or change dramatically in value upon firing, or the dielectric may become conductive to the point of catastrophic failure. The resultant resistors should be evaluated to determine if the electrical and physical properties are within the limits imposed by design.

2.8.1.1.2 Repetitive Firing - In some instances, due to reaction between resistors and dielectric, it may be advisable to print and fire the resistors on the bare substrate prior to print and fire build-up of the multilayer structure. The subsequent print and fire operations can in some instances, alter the electrical characteristics of the resistors due to multiple firing as compared to single firing. It is advisable to simulate the actual conditions that the end product will experience to determine the final result.

2.8.1.1.3 Geometry Sensitivity - The fired termination of thick film resistors consists of a complex diffusion of conductor and resistor compounds in the interface area. This diffusion or interface reaction is a major contribution to the geometry sensitivity of thick film resistors. This "as fired" resistivity for a specific geometry can be plotted as a nomograph to be used as a design standard of resistance versus size. A separate nomograph should be constructed for each specific combination of conductor and sheet resistivity of resistor.

Using the resistor test pattern, an evaluation of the electrical parameters of the finished resistors may be accomplished. The most significant factors to be considered are: (1) "as fired" sheet resistivity, (2) TCR, (3) VCR, (4) power stability and (5) drift. The resistor information form shown in Figure 2.8-2 can be used for resistor data acquisition.

X-335A RESISTOR TEST PATTERN — SAMPLE NO. _____

RESISTOR PASTE MFGR. —
VENDOR SPECIFIED SHEET RESISTIVITY (Ω/□) —
PASTE LOT NO. —
DATE FIRED —
FURNACE USED —
PEAK FIRING TEMP. —

CONDUCTOR PASTE MFGR. —
TYPE OF MATERIAL —
PASTE LOT NO. —
DATE FIRED —
FURNACE USED —
PEAK FIRING TEMP. —

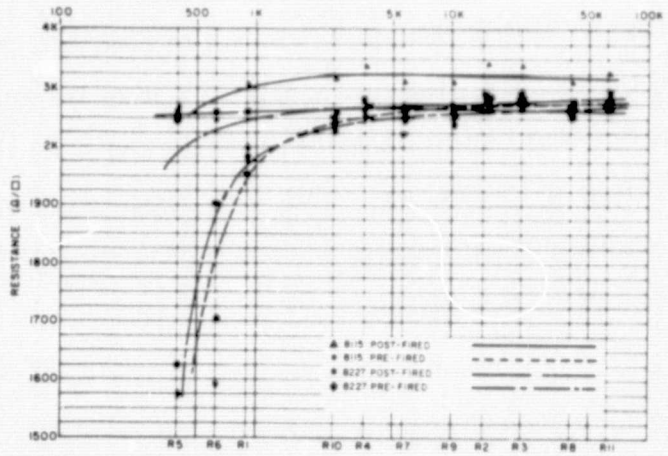
RESISTOR FIRING SEQUENCE: ☐ Before Conductor ☐ After Conductor

RES. NO.	DIMENSIONS (mils) W X L	AREA (Sq. Mils)	R@+25°C (Ω)	R@+125°C (Ω)	R@-25°C (Ω)	TCR (PPM/°C) +25°C to +125°C
1	30 x 30	900				
2	120 x 120	14,400				
3	150 x 150	22,500				
4	60 x 60	3,600				
5	20 x 20	400				
6	25 x 25	625				
7	75 x 75	5,625				
8	200 x 200	40,000				
9	100 x 100	10,000				
10	50 x 50	2,500				
11	250 x 250	62,500				
12	50 x 100 2 Parallel	2 (5,000 ea.)				

AVERAGE RESISTOR THICKNESS _____
AVERAGE SHEET RESISTIVITY (Ω/□) _____
OBSERVATIONS AND COMMENTS:

FIGURE 2.8-2. RESISTOR INFORMATION FORM USED TO ESTABLISH THE RELATIONSHIP BETWEEN RESISTOR SIZE TO "AS FIRED" RESISTANCE

Resistor Area (Square Mils)



EMCA 1kΩ/□

Test Resistors (See Figure 2.8-2)

FIGURE 2.8-3 Plot of the Typical Change in Resistance as a Function of Physical Size

2.8.1.2 Conductors

The conductors are critical circuit elements. The most common catastrophic failure mechanisms are shorts and opens with either one being potentially intermittent. The conductors, as in the case of resistors, may exhibit entirely different physical characteristics when printed on bare substrates as compared with printing on glazes or thick film dielectrics. The difference in characteristics may be a result of interreaction between conductor and dielectric materials or may result from the different surface topography of screen and fired dielectrics compared to bare substrates.

2.8.1.2.1 Bonding Pad Test Pattern

A conductor test pattern for evaluation of termination solder and bondability is shown in Figure 2.8-4. This test pattern consists of .050 x .100 and .025 x .100 inch conductors which can be deposited on bare substrates or on dielectric layers. A quantity of wires can be bonded to the conductor pads and then pull tested for evaluation. The following tests may prove useful for evaluation of materials and workmanship prior to circuit commitment.

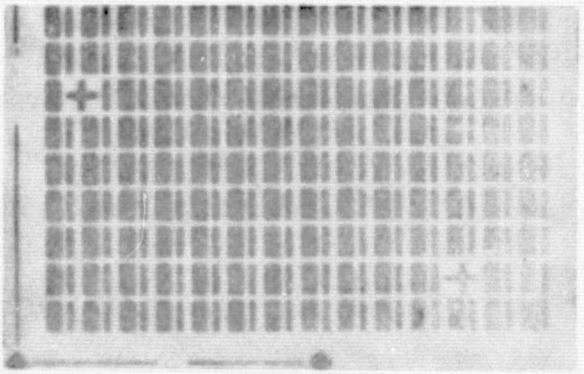


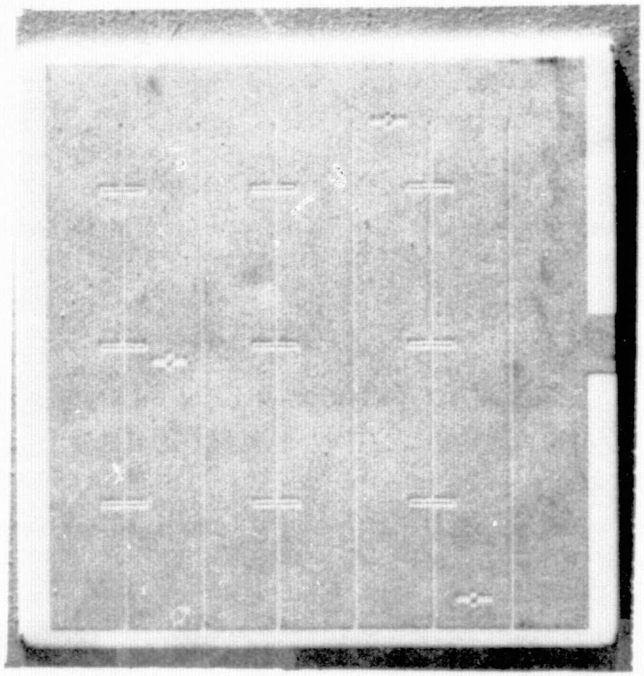
FIGURE 2.8-4. THICK FILM BONDING TEST PATTERN

2.8.1.2.1.1 Bondability - Some conductor materials may exhibit excellent bondability whether it be ultrasonic or thermocompression when deposited on bare substrates. However, when these same conductors are deposited over certain dielectrics or fired repeatedly, they may become impossible or difficult to bond.

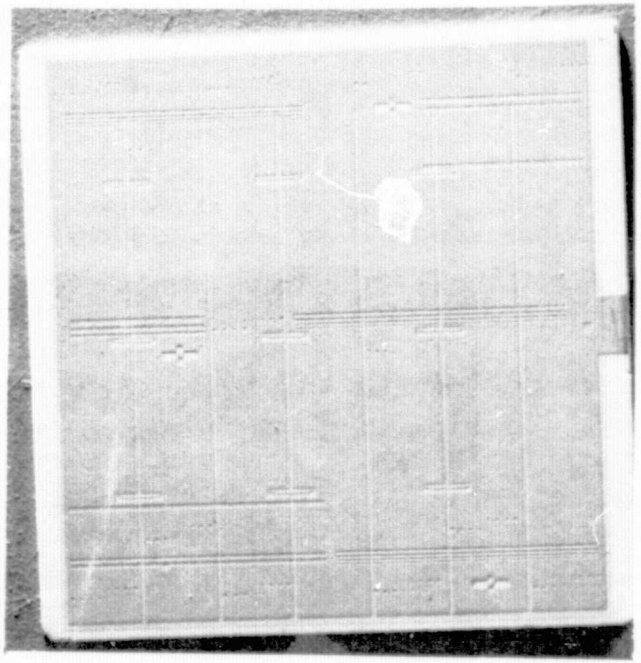
2.8.1.2.1.2 Soldering - Solderability can be adversely affected by deposition of certain conductors over dielectrics. It has also been found that repetitive firing can adversely affect the solderability by migration of glasses and/or formation of oxides on surface of conductors. This pattern can also be used to determine the detrimental effects of environment on the soldered or bonded joint integrity.

2.8.1.2.1.3 Die Brazing - The same conditions found to effect soldering can also be applied to die brazing.

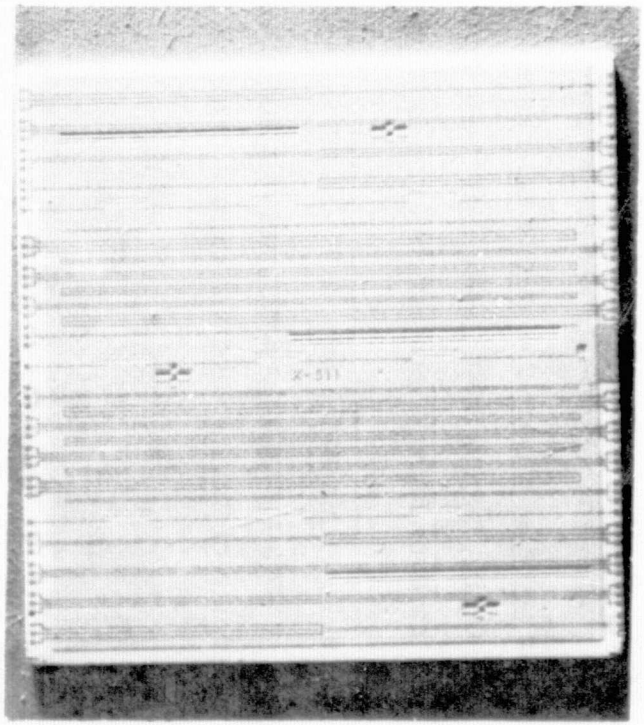
2.8.1.2.2 Interconnect Test Pattern - A fine line conductor/dielectric test pattern was developed during the materials study phase of this program. This pattern consists of a comb shaped ground or base plane, a dielectric layer incorporating groupings of patterns of round and square vias .002, .004, .006, .008, .010 and .012 inch diameter (or square), a top fine line conductor with groupings of interdigitated patterns of .002, .004, .006 and .008 inch width and spacing lines. This test pattern can be used to evaluate both conductor and dielectric materials and application workmanship. Shorts, opens and intermittents can be determined by probing the terminations after deposition and during environmental conditioning. An optical, as well as electrical, evaluation of this test pattern will determine the usability of the different combinations of conductor and dielectric materials. The samples shown in Figure 2.8-5 illustrate the three stages of the fine line test pattern fabrication.



Ground
Conductor



Isolation
Dielectric

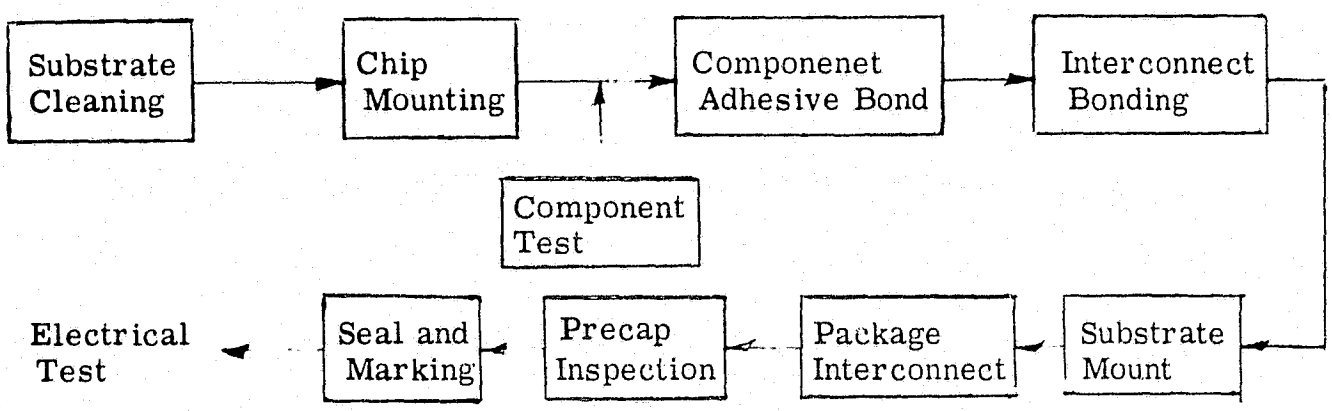


Top Interconnect
Conductor

FIGURE 2.8-5 FINE LINE TEST PATTER

2.9 Assembly Operations

The assembly operations include the efforts expended from the receipt of the probed and inspected substrate to the delivery of the sealed and inspected unit ready for electrical test. The assembly operations include functions which overlap in practice but for simplification, the following flow chart is representative.



Before assembly operations begin, complete detailed assembly drawings should be provided to the operator. All applicable process or instruction sheets should be provided and the operator should become familiar with the contents and the equipment being used. The operator should be proficient.

2.9.1 Substrate Cleaning

All substrates must be cleaned at the time of assembly. Contamination can have an adverse effect on all phases of the assembly operation. A standard cleaning operation includes detergent wash and rinse in deionized water followed by alcohol rinse with elevated temperature bake out to remove moisture.

2.9.2 Chip Mounting

Chip mounting refers to the mounting of active device chips mounted to a carrier or to the substrate itself prior to interconnect bonding. The two

methods most frequently used for active device chip mounting are eutectic die bonding and conductive or non-conductive epoxy bonding.

2.9.2.1 Eutectic Die Bonding

Eutectic die bonding is the attachment of a silicon device by the use of a preform of a eutectic alloy placed between the silicon chip and the gold metallization to which it is attached. When a preform is used, the device is positioned with the preform eutectic material between it and the metallization area while being heated to the melting temperature of the eutectic. A heated column is usually used in conjunction with a chip manipulation collet.

When a eutectic bond is formed between the device itself and the metallization, the device is forced against the metallization while the interface is brought to eutectic temperature by a heated stage and/or mechanical moving of the device to create heat. The device is usually held in a collet and ultrasonically scrubbed or hand manipulated. In some instances, the eutectic bond serves as an electrical connection to the device. The eutectic bond provides an excellent thermal path between the device and substrate.

2.9.2.2 Epoxy Bonding

Epoxy bonding is handled similarly to preform eutectic bonding except that a small quantity of conductive or non-conductive epoxy is used instead of a eutectic preform. The devices must not be disturbed until the epoxy has been cured and caution must be exercised to prevent epoxy contamination of any bond areas. Some fabrication facilities use conductive epoxy for the electrical and/or thermal bond. There exists considerable controversy concerning the reliability of conductive epoxy electrical bonds.

2.9.3 Component Adhesive Bonding

Components such as capacitors, device carriers, inductors and chip resistors can be assembled to the substrate using conductive or non-conductive epoxy. This operation is usually performed prior to interconnect bonding to the device. As in the case of die bonding with epoxies, conductive epoxy is sometimes used to make electrical as well as mechanical contact to the device.

A thorough investigation of the adhesive used and its structural integrity should be performed. Reliability of the hybrid assembly can be seriously affected by the choice of adhesives. The most common failure mechanisms found in adhesives include adhesion degradation after thermal exposure, decrease in continuity as a function of time and temperature (conductive epoxies) and electrolytic corrosion.

2.9.4 Interconnect Bonding

Interconnect bonding usually refers to the connection made from the device to the substrate which provides electrical continuity. The types of interconnect bonding include: (1) wire bonding, (2) beam lead and (3) special application interconnects.

2.9.4.1 Wire Bonding

The interconnect wire bonding used in the fabrication of multilayer hybrids include thermocompression nail head and stitch bonding, ultrasonic wire bonding and parallel gap welding.

2.9.4.1.1 Thermocompression Bonding

Thermocompression bonding can be accomplished with either a constant temperature bonder or pulse heated tip bonder. Several configurations of bonders are commercially available and should be investigated before a decision is made to incorporate a particular one into an assembly facility. The thermocompression bond can be of the nail head or stitch configuration. Normally, nail head bonds are made to the substrate metallization while stitch or wedge bonding is made on discrete components such as lid carriers and capacitors. A capillary tip is required for nail head bonding where a capillary or wedge tip can be used for stitch bonding. It is recommended that a double stitch bond be used to insure bond integrity after removing the wire end

Normally .001 inch diameter gold wire is used in thermocompression bonding but wire sizes from .007 inch diameter to .0015 inch diameter wire are used in some applications.

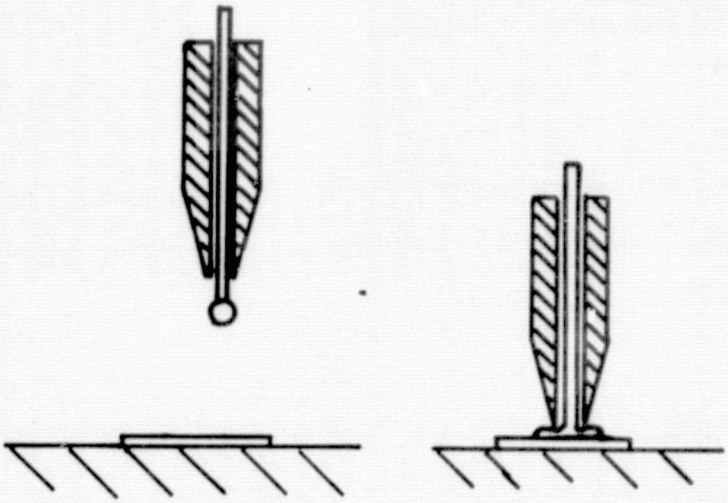


FIGURE 2.9-1
FORMING A NAILHEAD BOND WITH A CAPILLARY TIP BONDER

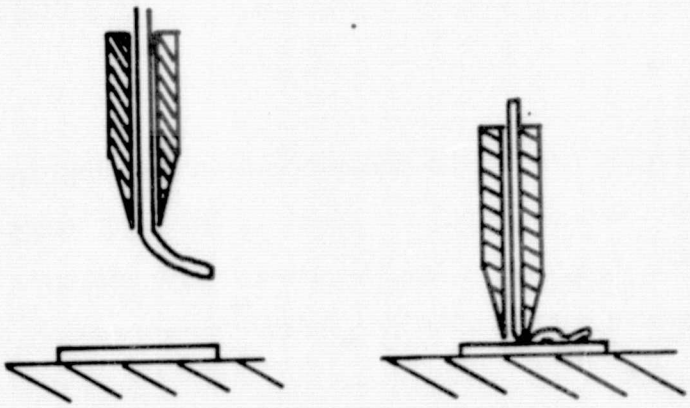


FIGURE 2.9-2
FORMING A STITCH BOND WITH A CAPILLARY TIP BONDER

2.9.4.1.2 Ultrasonic Wire Bonding

Ultrasonic wire bonding is required where aluminum wire is used as an interconnect. The bonding method is similar to thermocompression bonding with the exception that the bonding energy is supplied by ultrasonically scrubbing the wire into the metallization to which it is to be bonded.

2.9.4.1.3 Parallel Gap Bonding

Parallel gap bonding is used where larger wires and ribbons are required for interconnects. A pair of electrodes are used to pass a current through the wire while exerting a force to the bonding area.

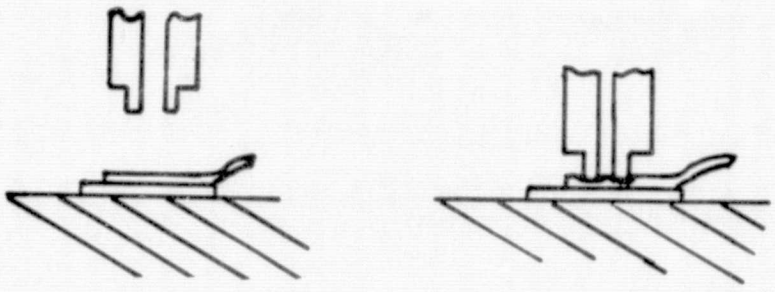


FIGURE 2.9-3 PERFORMING A PARALLEL GAP BOND

2.9.4.2 Beam Lead Bonding

Beam lead bonding is becoming one of the most common bonding methods used in multilayer circuit assembly. Several varieties of bonders are commercially available for accomplishing beam lead bonding. The methods used most frequently for bonding beam lead devices are thermocompression wedge bonding and "whole" head bonding.

2.9.4.2.1 Thermocompression Beam Lead Bonding

This type of bonding is similar to thermocompression wedge wire bonding where each beam is individually bonded to the substrate metallization using a thermocompression bonder. This method of bonding, while producing excellent end results, is difficult to accomplish as it is difficult to hold the beam lead device in the correct position while performing the bonding operation.

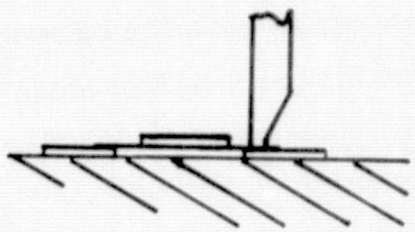


FIGURE 2.9-4
THERMOCOMPRESSION WEDGE BONDING BEAM LEADS

2.9.4.2.2 Wobble Head Bonding

This method of bonding utilizes a head which fits around the body of the beam lead device and over the beams protruding from the body. The bonding operation is performed by the head exerting pressure around the device in a wobbling motion to bond each beam individually. Excellent results can be obtained from a "wobble head" bonder used by an experienced operator. The use of a wobble head bonder requires uniformity of physical dimensions such as land or lead thickness.

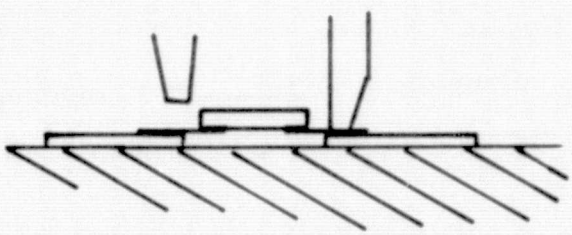


FIGURE 2.9-5
WOBBLE HEAD BONDER OPERATION

2.9.4.3 Special Application Bonding

The special application bonding includes flip chip bonding controlled collapse bonding and "spider" bonding. These types of bonding methods are not recommended for use in complex multilayer circuit fabrication.

2.9.5 Substrate Mounting

The substrate can be mounted into the package either before or after substrate assembly. It has been found that for most applications, assembly should be performed as completely as possible before commitment to the package. The substrate can be mounted in the package using conductive or non-conductive adhesives or by eutectic or solder attachment where backside metallization permits. Choice of mounting materials and methods can be a critical factor in reliability. A mismatch in the expansion characteristics of the substrate, package and mounting media can result in catastrophic failure in the package and/or substrate.

2.9.6 Package Interconnect

After attachment of the substrate to package, interconnect bonds can be performed and, if required, substrate component bonds performed.

2.9.7 Pre-cap Inspection

A precap visual and electrical inpsection should be performed to assure that the device meets the mechanical and electrical specifications under which it was designed. Workmanship standards should be critically observed and any rework necessary should be performed.

2.9.8 Sealing

Package sealing involves several different methods which are dependent upon circuit application and/or customer requirements. The basic types of sealing are:

1. Hermetic sealing using eutectic preforms
2. Hermetic reflow solder sealing
3. Package encapsulation using plastic materials

Package types include:

1. All metal with glass beads around leads
2. All ceramic
3. Combination ceramic/metal
4. Custom metal or plastic

The most prevalent sealing method involves either eutectic preforms or reflow solder sealing. Both manual and automatic sealing processes have been developed for both of the above mentioned techniques.

Prior to sealing, a complete cleaning and preseal visual inspection are required of each package. Before flatpack tinning an ultrasonic cleaning operation is recommended after which tinning is accomplished using a mildly activated flux and a solid 63 - 37 solder (melting point of 180 degrees centigrade). For eutectic sealing, an 80 - 20 gold tin preform with a melting point of 280 degrees centigrade is used. Removal of flux prior to sealing is important. Cleaning is accomplished with special solvents and thorough rinsing techniques followed by drying with dry nitrogen.

A two hour vacuum bake at 125 degrees centigrade at greater than 25 inches mercury is recommended prior to sealing. Before the circuit is removed from the oven, the oven must be allowed to cool below 40 degrees centigrade before the vacuum is released. A nitrogen/helium dry box atmosphere is recommended 30 minutes before sealing. The helium must be approximately 25 percent of the nitrogen/helium atmosphere. The dry box exit water vapor is monitored and is not allowed to exceed 60 ppm during sealing operations.

Other sealing parameters include hot plate temperatures and deviations. fixture alignment dimensions, time of direct contact heating and forces to be used. Inspection criteria includes quantity of solder at the seal, position of cover on header, leaks that may be visually detected. etc.

Rework of sealed packages is possible on reflow solder sealed units only. This type of package can be opened, the assembly reworked and the package resealed. Rework of the seal area is done in a dry box atmosphere using a heated tool.

2.9.8.1 Leak Testing

A gross leak test for prototype modules consists of placing the module or flatpack in a beaker of demineralized water at 90 degrees $\pm$ 5 degrees centigrade; the escape of gas bubbles from the package indicates a gross leak. If no bubbles appear from the package after a minimum of three minutes immersion, it is removed from the beaker and blown dry with a jet of dry nitrogen at a maximum of 40 PSIG.

Fine leak tests are performed in accordance with MIL-STD-202C, Method IV except that upon completion of the test procedure, the specimen should not be rechecked for gross leaks. Unless otherwise specified by the customer, a leak rate not greater than 6×10^{-8} cc/sec should be considered acceptable for hermetic seal. Packages being tested are not subjected to a pressure level greater than 1×10^{-5} Torr; the pressure level is maintained until the leak indicator meter has stabilized. Additional leak tests are performed on packages as may be necessary.

2.9.9 Marking

The package marking should be impervious to moisture and solvents and resistant to abrasion. The marking inks which seem most applicable are the two part or single component epoxy inks. The methods of application of marking inks includes screen printing, spray stencil and hand application.

2.10 Inspection and Test Procedures

The inspection and test procedures which apply to multilayer ceramic circuits can be grouped into two sections, process related testing and functional circuit inspection or pre-cap inspection as it is commonly referred to.

2.10.1 Process Testing

Process Testing includes testing of materials and their application to the substrate fabrication and assembly. Each step in the process flow is important in the fabrication of a hybrid microcircuit. High confidence level must be established and maintained in operator and process functions through monitoring by well trained Quality Control personnel. Adequate inspection points should be established to exercise quality control with normal inspections. Intermediate inspection points are imposed in the event of problems evidenced in normal inspection or where expedient to adequate control of certain unique circuits or assemblies.

The critical inspection points may be listed as follows:

1. Receiving Inspection

   Components and materials are inspected to insure conformance with the physical requirements of the material specifications under which they were purchased. Material testing is accomplished either at the incoming inspection clean room station or at the applicable user area under the direction of the Quality Control inspector.

2. Film Mask Inspection

   All reduced photographic masks are inspected to insure compliance with the master artwork requirements and the design specifications under which it was generated.

3. Thick Film Circuit Inspection

   All screened and fired circuits are back lit optically inspected to insure compliance with processes and design specifications under which they were fabricated. Particular attention is given to potential problem areas such as possible shorts or opens, sparse

metallization or dielectric and harmful misregistration. The physical characteristics of the fabricated substrate are carefully monitored to insure compliance with the mechanical and electrical requirements of the completed assembly.

4. Fabrication Materials

Controls should be imposed wherever necessary, to insure maximum performance in all processes. These generally are substantiated by test data with surveillance by Quality Control.

Certain materials are subjected to laboratory evaluation prior to acceptance by Receiving Inspection. For example, interconnect wire is inspected for contamination by the Microelectronics Laboratory and thick film pastes are evaluated by the Thick Film Laboratory for resistivity, viscosity, and fired adhesion. Some discrete components are tested for bondability by the Microelectronics Laboratory.

Thick film depositions should be logged listing materials used and the firing temperature cycle. Adhesion samples are tested as a regularly scheduled process function. Furnace temperature profiles are recorded at scheduled intervals. Deposited resistors are individually tested and trimmed as necessary. Resistor characteristic information is recorded as a function of process documentation. Epoxies used as adhesives require periodic shear testing with mechanical samples. These samples are oven cured along with production assemblies using the same epoxy batch.

5. Machine Bonds

Machine bonds should be sample tested at the beginning of each shift. Included are ultrasonic, thermocompression, parallel gap, and pincer type wire bonds. Die brazing, flip chip, and beam lead bonds are similarly tested. Pull tests or shear tests, appropriate

to the device, are used for this purpose. These scheduled tests serve to verify machine performance in conformance with initial qualification and iso-strength certifications.

6. Process Specifications

Process Specifications should define all processes and establish requirements and tests necessary to insure the production of quality hybrid microcircuits. All processes are evaluated by reliability testing.

A process record should accompany each device being fabricated. Each operation including any repairs, inspection and test, is detailed on this tag for immediate reference as well as a permanent record.

7. Environmental Testing

The materials used in the fabrication should be tested to assure their abilities to meet the environmental specifications imposed on the end product. The materials should be evaluated by use of suitable test patterns to determine their integrity in environments such as thermal and mechanical shock, temperature cycling, moisture and vibration.

2.10.2 Pre-cap Inspection

All completed multilayer circuit assemblies should be inspected prior to the sealing operation to insure structural and electrical integrity. Particular attention is paid to workmanship and compliance with assembly process documents. A major portion of circuit failures can be prevented by a stringent inspection at this point.

2.10.2.1 Apparatus

The equipment and apparatus for this test shall include an optical microscope capable of examination at the specified magnifications, handling fixtures,

and any visual aids (e.g., gages, design drawings, cameras, etc.) necessary to perform an effective examination and enable the operator to make objective decisions concerning the acceptability of the device being examined.

2.10.2.2 Procedure

2.10.2.2.1 General

The device shall be examined in a suitable sequence of observations within the specified magnification range to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition.

2.10.2.2.1.1 Sequence of Inspection

The order in which criteria are presented is not a required order of examination and may be varied at the discretion of the manufacturer. Where inverted mounting technologies are employed, the inspection criteria contained herein that cannot be performed after mounting shall be performed prior to attachment to the substrate.

2.10.2.2.1.2 Inspection Control

In all cases, examination prior to die or substrate attachment shall be performed under the same control and supervision that is required at the final preseal inspection station. Proper control shall be exercised after inspection to insure that the hybrid circuits are stored in an inert, dry, dust-free environment.

2.10.2.2.1.3 Magnification

Unless other wise specified, all examinations shall be performed at a magnification of 30X to 60X. When a reference document is required, the magnification specified in the reference document shall be used.

2.10.2.2.1.4 Illumination and Viewing Angle

Inspection shall be performed with both vertical and oblique illumination. The examination may be performed using either vertical or oblique viewing angles.

2.10.2.2.1.5 Applicable Documents

MIL-STD-883; Test Methods for Microelectronics
Method 2010.2, Internal Visual (Pre-Cap)

MIL-C-55681A; Capacitors, Chip, Multiple Layer, Dixed, Unencapsulated, Ceramic Dielectric, Specification for

MIL-R-55342A; Resistors, Chip, Fixed Film, Specification for

2.10.2.2.2 Examination Requirements

2.10.2.2.2.1 Semiconductor Chip Devices

All semiconductors shall be inspected in accordance with the applicable test conditions of MIL-STD-833, Method 2010.2.

2.10.2.2.2.2 Passive Chip Devices

All passive chip devices shall be inspected in accordance with the visual criteria of the applicable specification listed in 3.1.5.

2.10.2.2.2.3 Substrate Films

Any of the following defects shall be cause for rejection.

2.10.2.2.2.3.1 Conductors

a. A scratch(s), nick(s), or void(s) greater than 50 percent of the design width (see Figure 2-10.1).

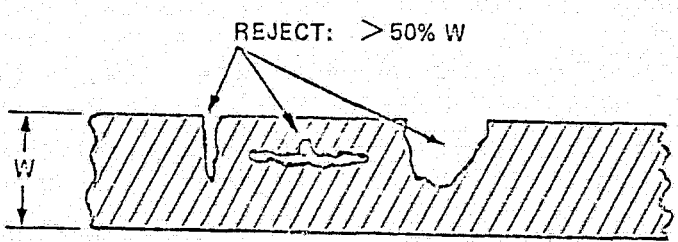


FIGURE 2-10.1

b. Lifting, peeling or blistering (see Figure 2.10-2).

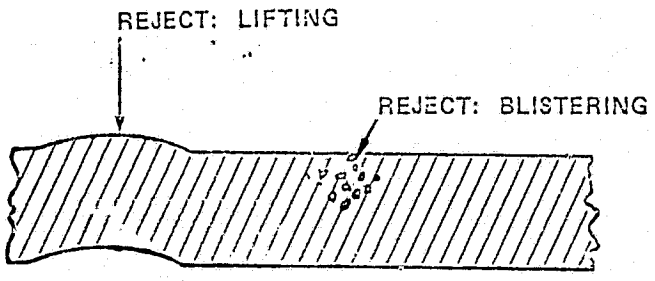


FIGURE 2.10-2

c. A protrusion or expansion of the conductor that reduces the distance to another circuit element by more than 50 percent of the design separation (see Figure 2.10-3).

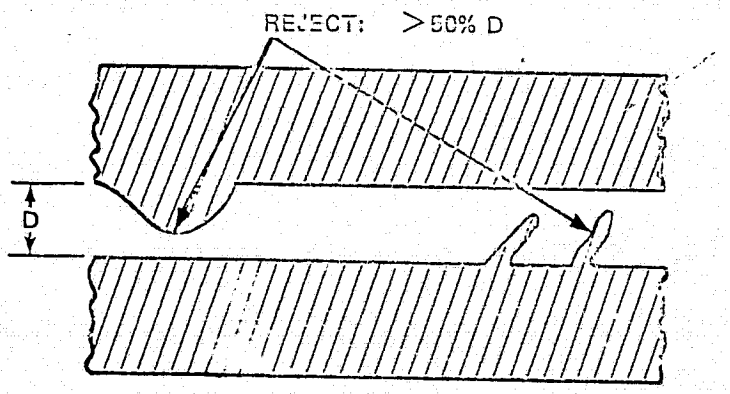


FIGURE 2.10-3

d. A particle or foreign material greater than 50% of the design width or .005 inch (see Figure 2.10-4).

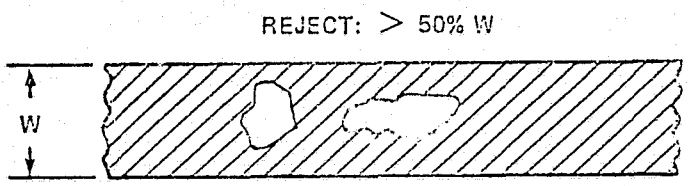


FIGURE 2.10-4

e. Except for wrap-around and lead frame bonding areas, distance between the conductor and the edge of the substrate less than .010 inch for thick films (see Figure 2.10-5).

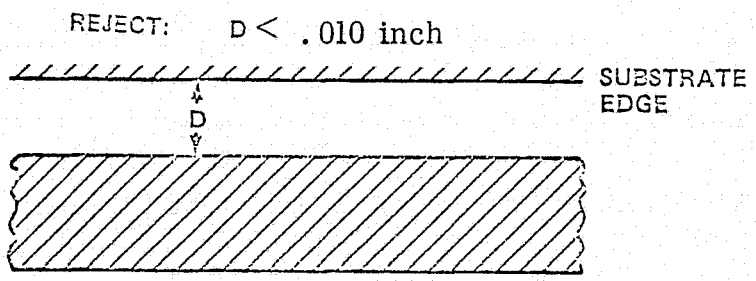


FIGURE 2.10-5

f. Misalignment where conductor interface is less than 50 percent of the narrower conductor (see Figure 2.10-6).

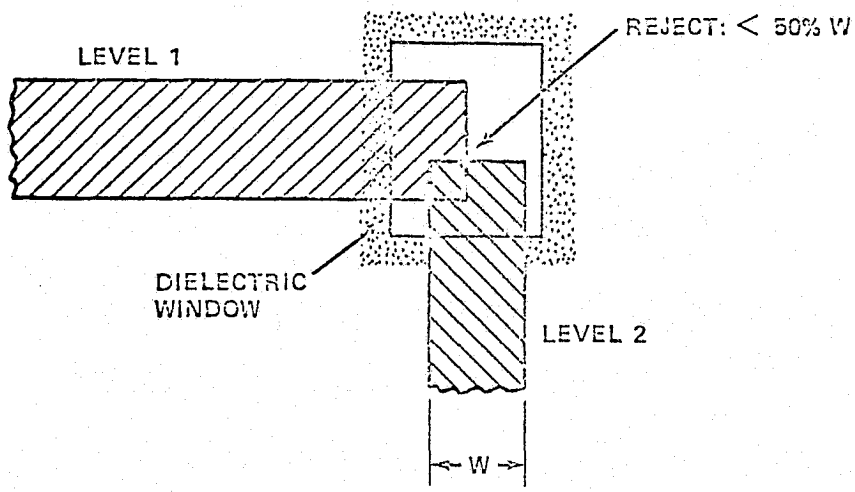


FIGURE 2.10-6

g. Evidence of nonuniformity in color or contamination such as flux residue, corrosion, etc.

2.10.2.2.2.3.2 Resistors

a. A scratch(s), nick(s), or void(s) greater than 50 percent of the design width (see Figure 2.10-7).

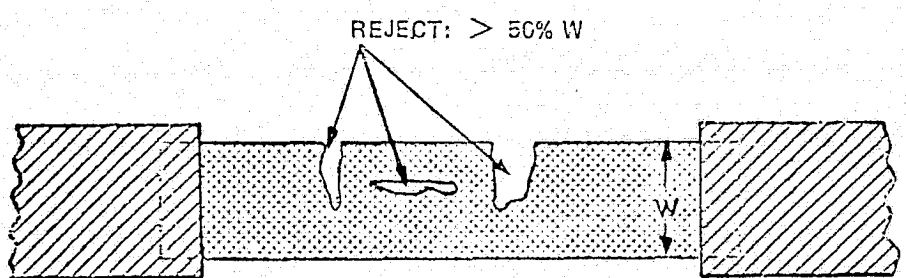


FIGURE 2.10-7

b. Lifting, peeling or blistering (see Figure 2.10-8).

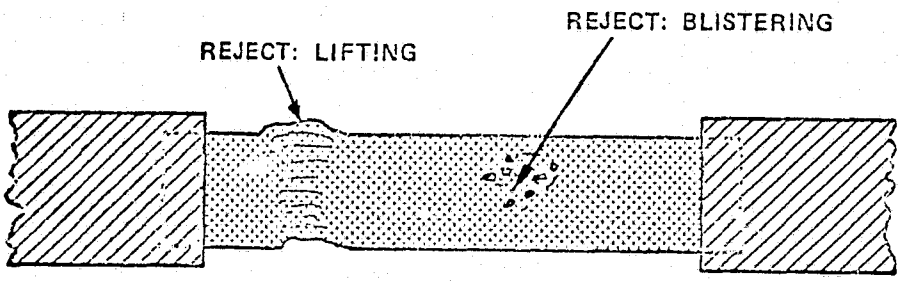


FIGURE 2.10-8

c. A protrusion or expansion of the resistor that reduces the distance to another circuit element by more than 50 percent of the design separation (see Figure 2.10-9).

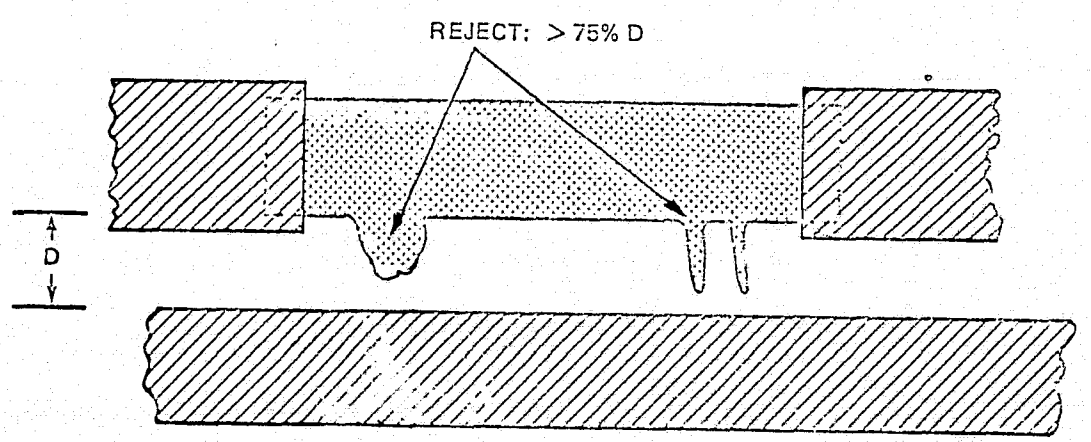


FIGURE 2.10-9

d. A particle or foreign material greater than 50 percent of the design width or .005 inch (see Figure 2.10-10).

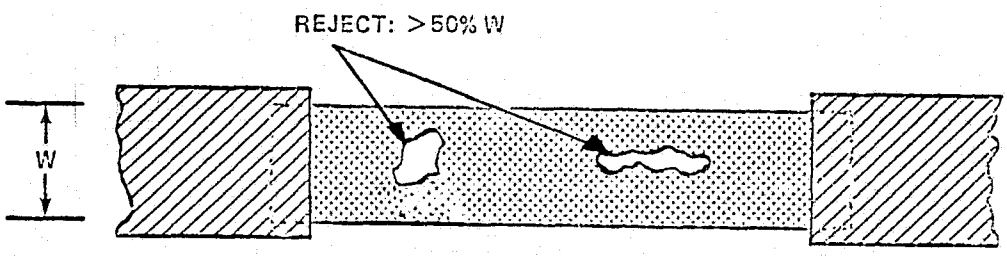


FIGURE 2.10-10

e. Distance between the edge of the resistor and the edge of the substrate less than .010 inch. (See Figure 2.10-11.)

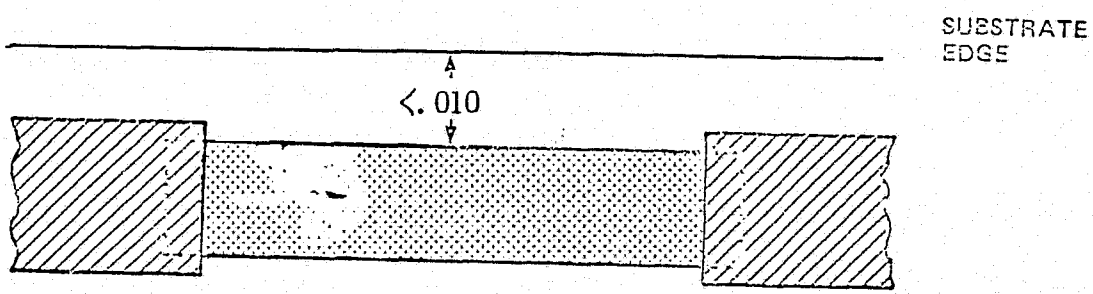


FIGURE 2.10-11

f. Distance between the edge of the resistor and an adjacent circuit element less than .010 inch for thick films (see Figure 2.10-12).

Reject: D < .010 inch

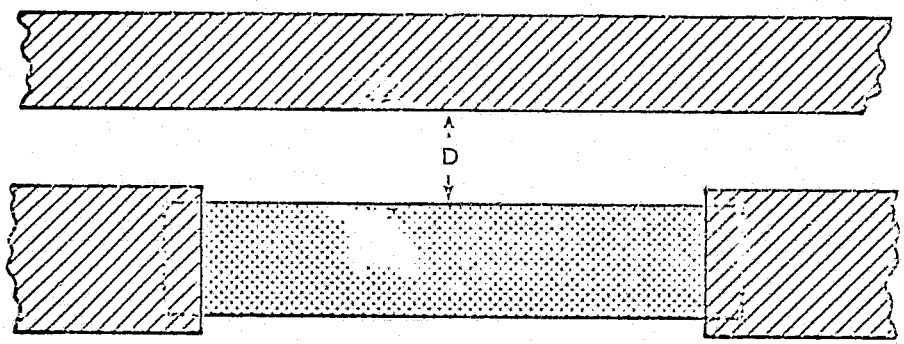


FIGURE 2.10-12

g. Evidence of nonuniformity in color or contamination such as flux residues, corrosion, etc.

h. Misalignment where a resistor is not 100 percent terminated by conductor (see Figure 2.10-13).

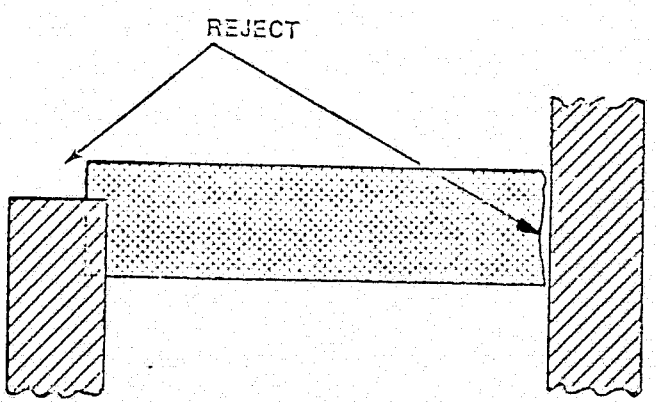


FIGURE 2.10-13

i. A trim-cut greater than 50 percent of the design width. NOTE: A scratch, nick, or void opposite a 50 percent trim-cut is cause for rejection (see Figure 2.10-14).

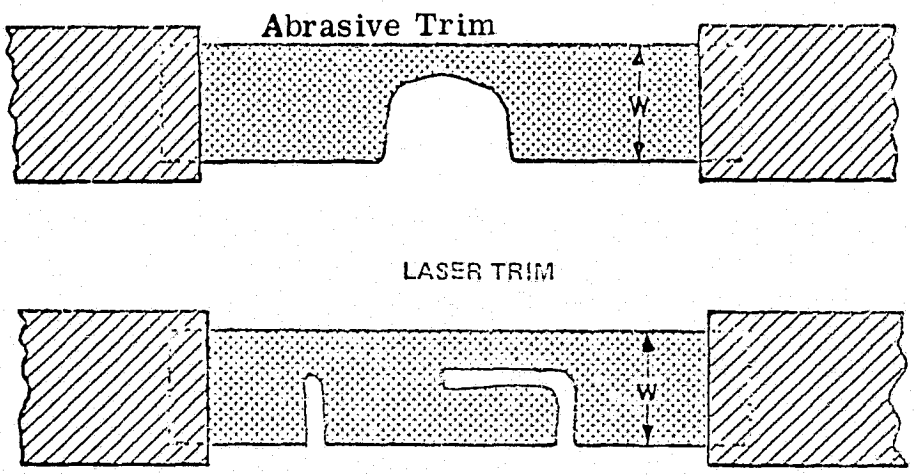


FIGURE 2.10-14

j. Evidence of microcracking or a severe heat effected zone around the trim-cut edge (see Figure 2.10-15).

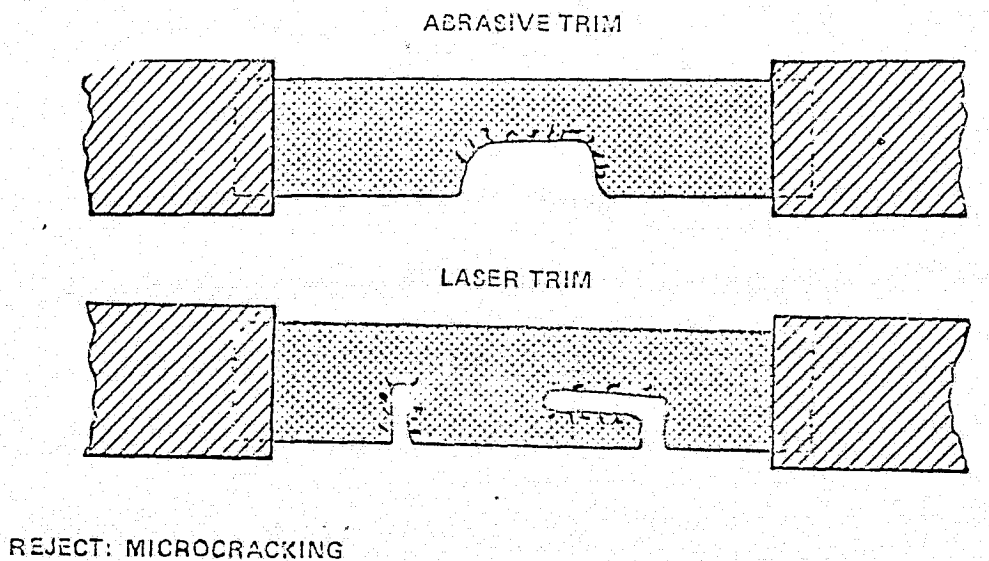


FIGURE 2.10-15

k. Residue in the trim kerf or failure to scour the trim-cut to the substrate (see Figure 2.10-16).

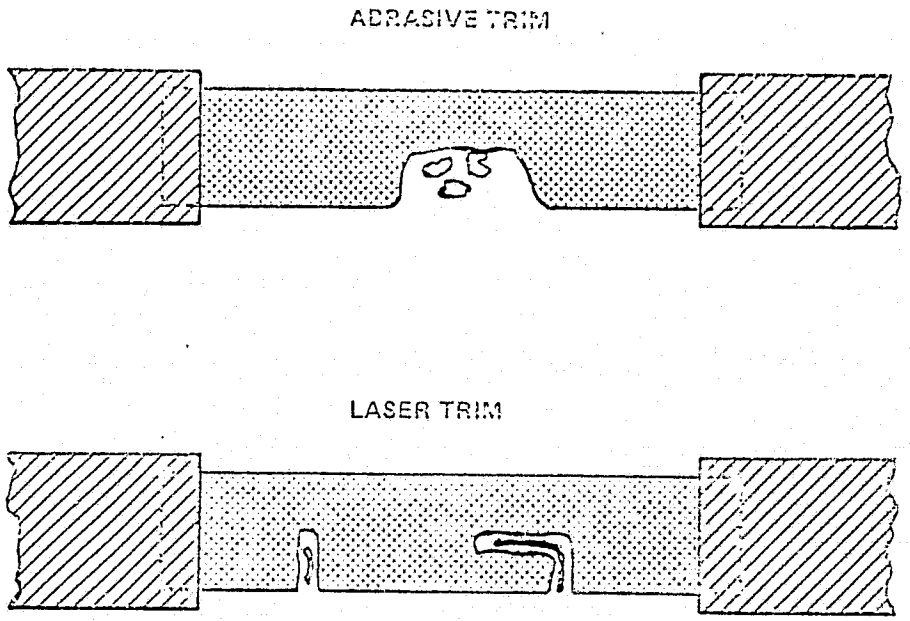


FIGURE 2.10-16

2.10.2.2.2.3.3 Dielectric Overglaze

a. A scratch(s), nick(s), or void(s) that exposes more than 50 percent of the buried elment design width (see Figure 2.10-17).

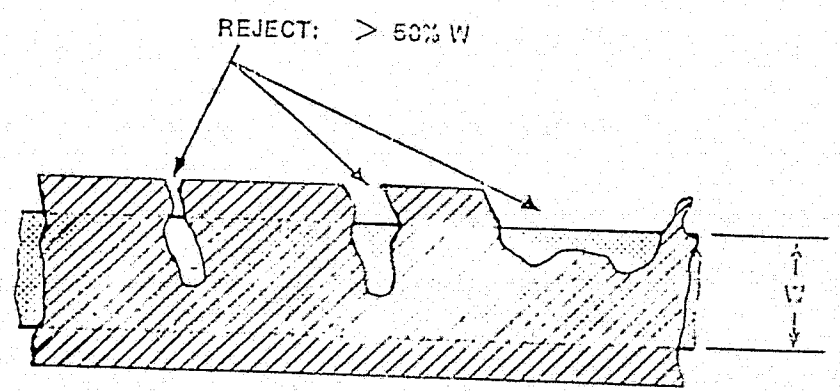


FIGURE 2.10-17

b. Lifting, peeling, blistering, or crazing (see Figure 2.10-18).

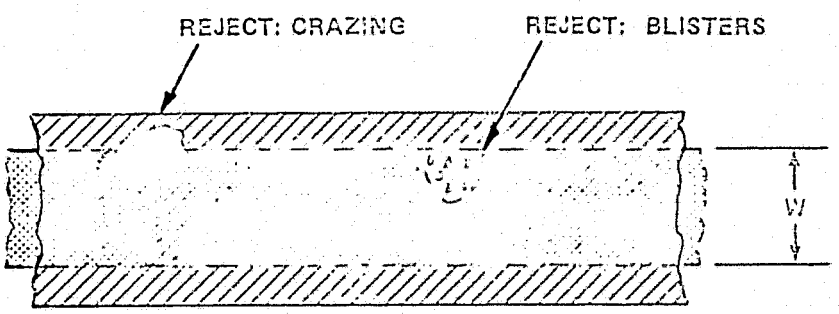


FIGURE 2.10-18

c. A particle or foreign material greater than 50 percent of the buried element design width or .005 inch (see Figure 2.10-19).

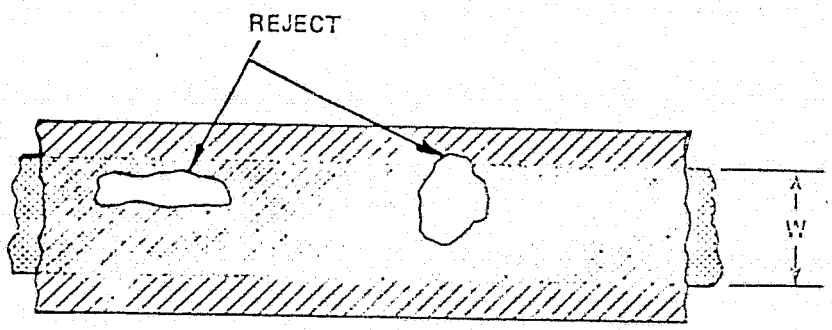


FIGURE 2.10-19

d. Any dielectric material covering bonding or soldering area (see Figure 2.10-20).

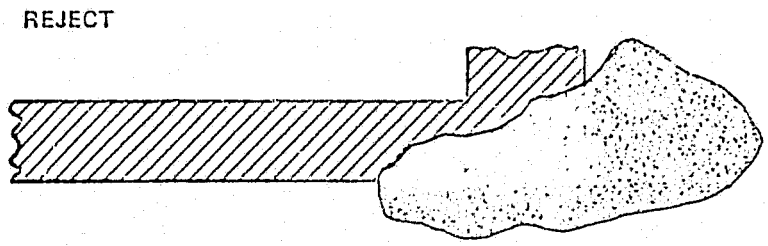


FIGURE 2.10-20

e. Evidence of nonuniformity in color or contamination such as flux residues, corrosion, etc.

2.10.2.2.2.3.4 Dielectric Crossover

a. Dielectric coverage less than .005 inch beyond the edge of any metallization crossover (see Figure 2.10-21).

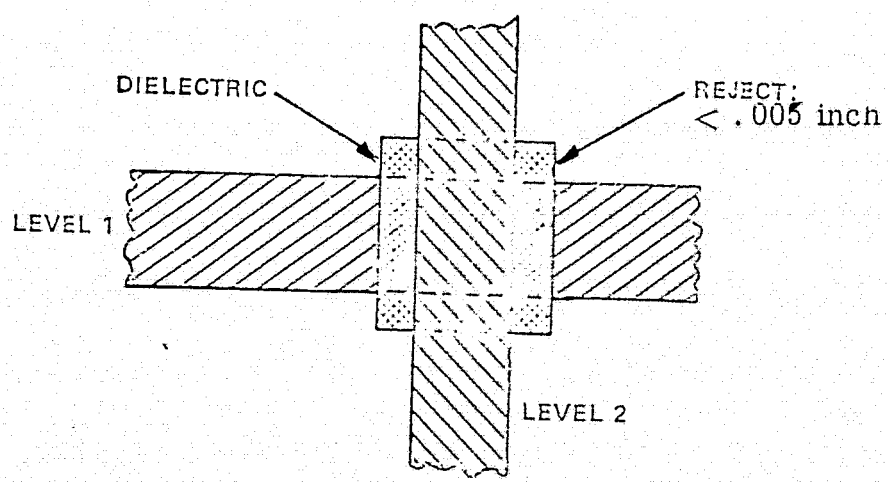


FIGURE 2.10-21

b. A scratch(s), nick(s), void(s) or particle(s) within .005 inch of the edge of any metallization crossover (see Figure 2.10-22).

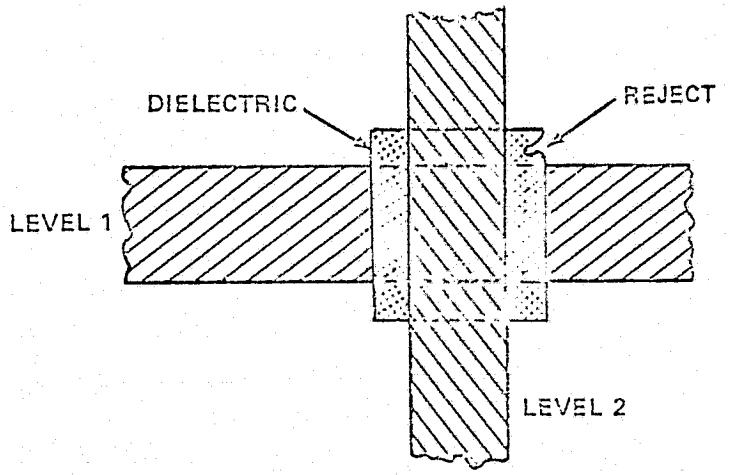


FIGURE 2.10-22

c. Evidence of nonuniformity in color or contamination such as flux residues, corrosion, etc.

2.10.2.2.2.4 Substrate Defects

Any of the following shall be cause for rejection (see Figure 2.10-23).

a. A blister or peak extending above the glaze surface (see "a" of Figure 2.10-23).

b. A crack (see "b" of Figure 2.10-23).

c. A particle or foreign material greater than .003 inch diameter (see "c" of Figure 2.10-23).

d. A chip-out or nick greater than .005 inch (see "d" of Figure 2.10-23).

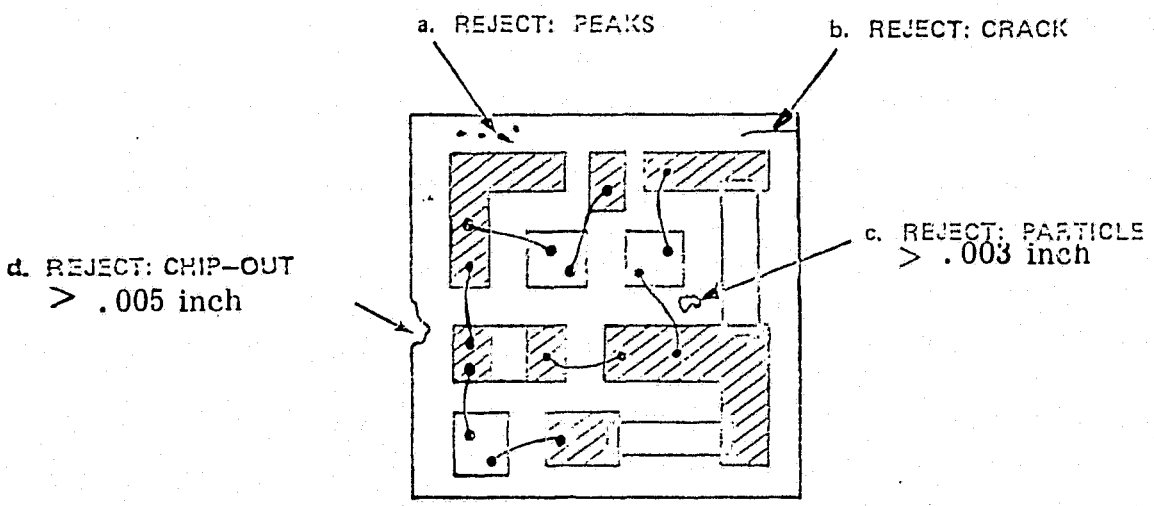


FIGURE 2.10-23

e. Evidence of nonuniformity in color or contamination such as flux residues, corrosion, etc.

2.10.2.2.2.5 Component Attachment to Substrate

Any of the following shall be cause for rejection for solder, epoxy, and eutetic attachments:

a. Mounting material build up that extends above or touches the top surface of the component (see Figure 2.10-24).

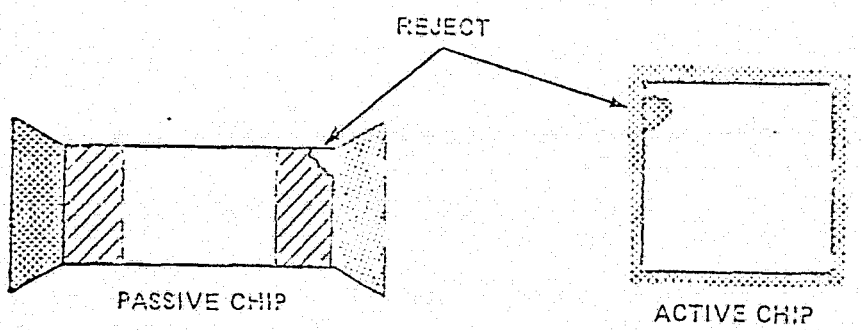


FIGURE 2.10-24

b. Balling or flaking of the mounting material (see Figure 2.10-25).

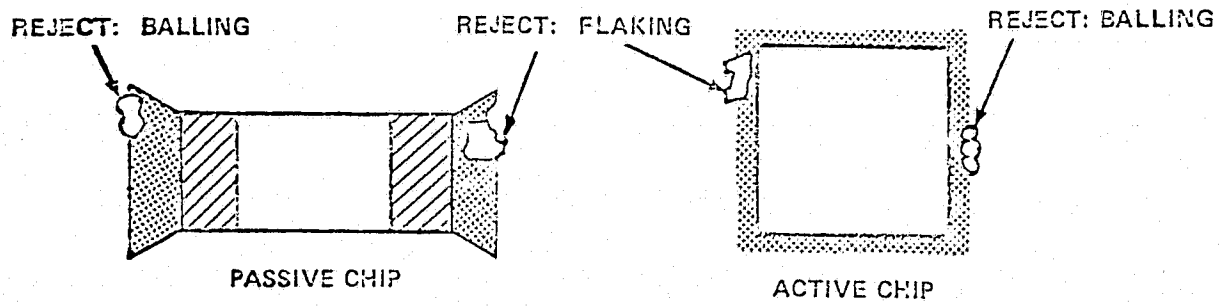


FIGURE 2.10-25

c. A crack or pit in the mounting material (see Figure 2.10-26).

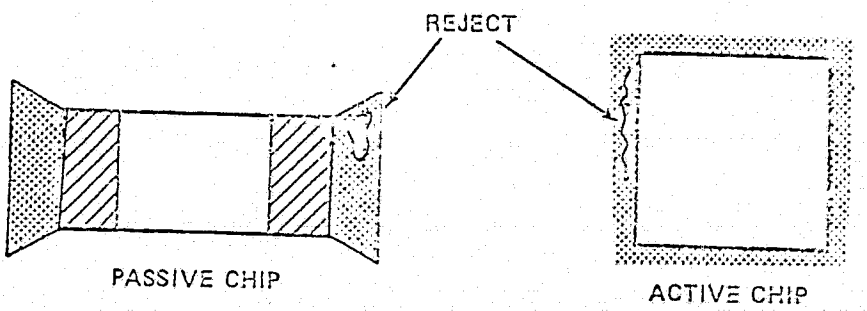


FIGURE 2.10-26

d. Less than 75 percent continuous wetting around the termination perimeter of active and passive chips (see Figure 2.10-27).

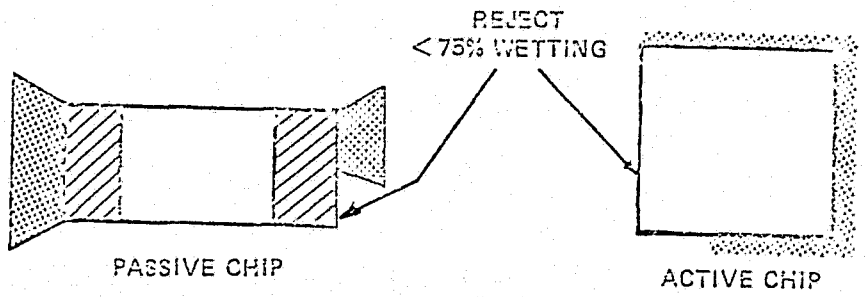


FIGURE 2.10-27

e. Evidence of nonuniformity in color, texture, or contamination of the mounting material.

2.10.2.2.2.5 Substrate Attachment to Packages

Any of the following shall be cause for rejection for solder, epoxy, and eutectic attachments:

a. Mounting material build up that extends above or rouches the top surface of the substrate (see Figure 2.10-28).

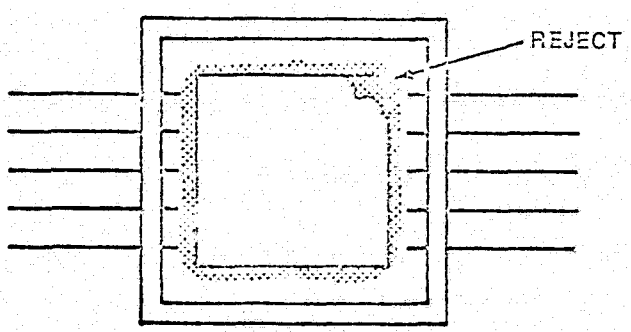


FIGURE 2.10-28

b. Balling or flaking of the attachment material (see Figure 2.10-29).

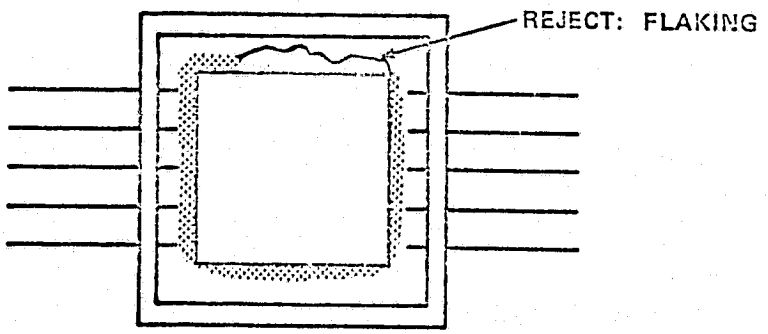


FIGURE 2.10-29

c. A crack or pit in the mounting material (see Figure 2.10-30).

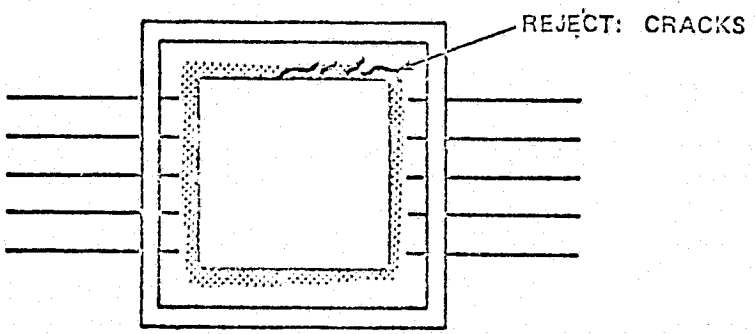


FIGURE 2.10-30

d. Less than 75 percent continuous wetting around the substrate perimeter (see Figure 2.10-31).

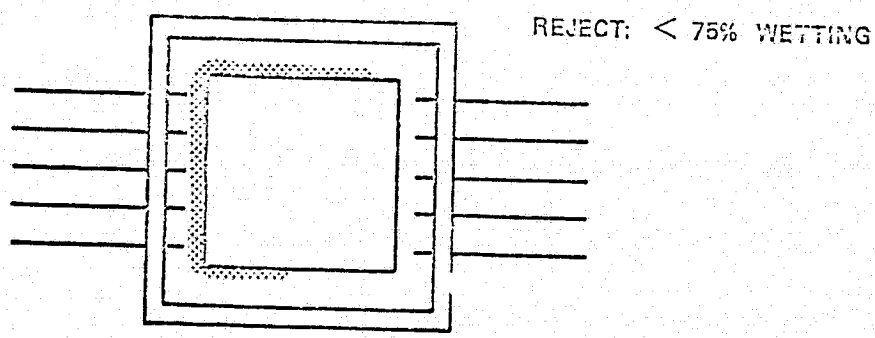


FIGURE 2.10-31

e. Evidence of nonuniformity in color texture or contamination of the mounting material

2.10.2.2.2.7 Wire Bonds

All wire bond inspections shall be performed using both vertical and oblique viewing angles.

2.10.2.2.2.7.1 General (Gold Ball and Wedge)

The following shall be cause for rejection:

a. Bond(s) on the die where less than 75 percent of the bond is within the unglassivated bonding pad area for class A circuits and 50 percent for class B and C circuits.

b. Bond(s) on the package post which are not completely within the boundaries of the package post.

c. Bond(s) placed so that the separation between two bonds or the bond and the operating metallization not connected to it is less than .002 inch (see Figure 2.10-32).

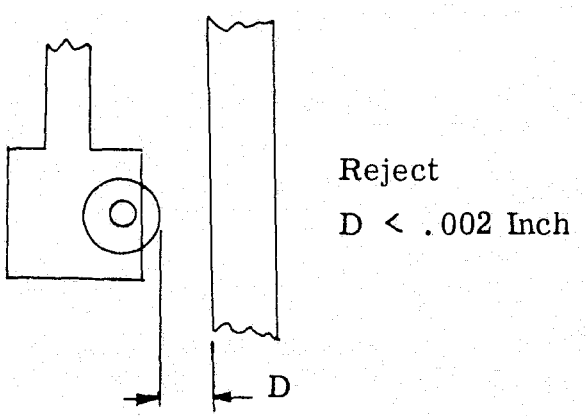


FIGURE 2.10-32

d. Wire bond tail(s) which extend over or make contact with any metallization not covered by glassivation and not connected to the bond area (see Figure 2.10-33).

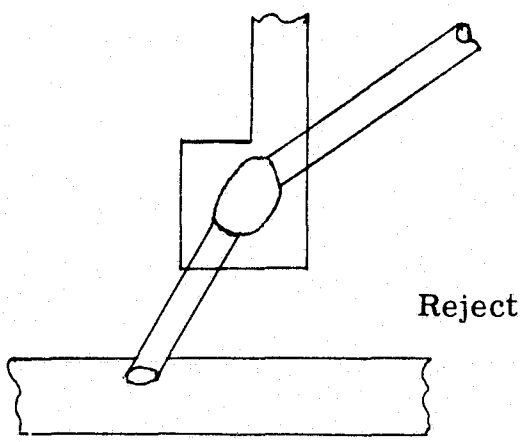


FIGURE 2.10-33

e. Tearing bond(s) at single bond locations where less than 50 percent of the bond impression remains attached (see Figure 2.10-34).

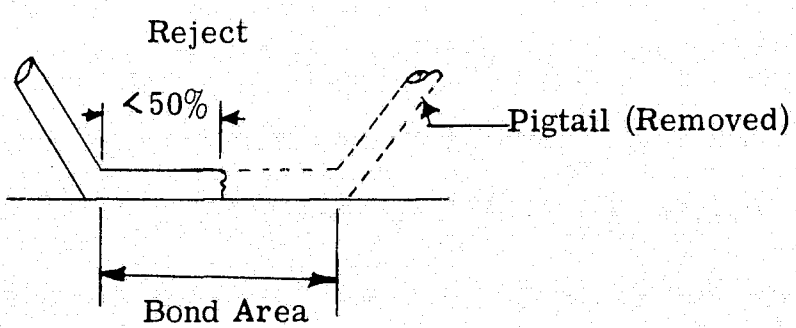


FIGURE 2.10-34

f. Any intermetallic formation extending the periphery of any gold bond.

g. Bond(s) in the fillet area (or the point where metallization exits from the bonding pad) which do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the fillet or one side of the connecting metallization pad (see Figure 2.10-35).

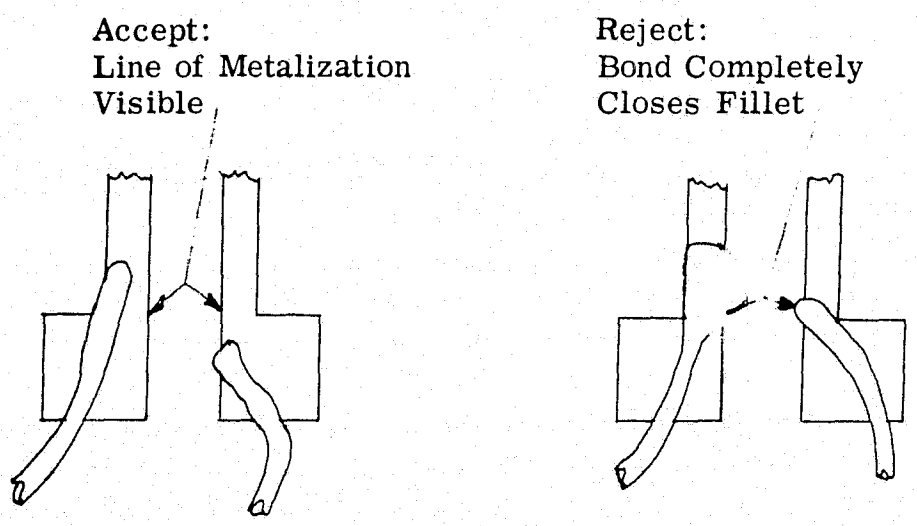


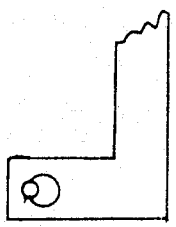
FIGURE 2.10-35

2.10.2.2.2.7.2 Gold Ball Bonds

The following shall be cause for rejection:

a. Gold ball bond(s) on the die or package post where the ball bond diameter is less than 2.0 times or greater than 6.0 times the wire diameter.

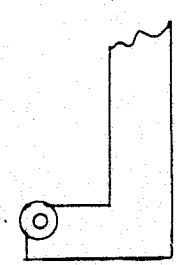
b. Gold ball bond(s) where the wire exit is not completely within the periphery of the ball (see Figure 2.10-36).



Reject:
Wire Exit Not in
Periphery of Ball

FIGURE 2.10-36

c. Gold ball bond(s) where the wire exit is not within the boundaries of the bonding pad (see Figure 2.10-37).



Reject:
Wire Exit not within
Bonding Pad Boundry

FIGURE 2.10-37

2.10.2.2.2.7.3 Wedge Bonds

The following shall be cause for rejection:

a. Ultrasonic wedge bonds on the die, substrate, or package post whose width is less than 1.2 times or greater than 2.5 times the wire diameter.

b. Thermocompression wedge bonds on the die, substrate, or package post whose width is less than 2.0 times or greater than 3.0 times the wire diameter.

2.10.2.2.2.7.4 Beam-Lead Bonds

The inspection criteria specified shall apply to the completed bond area made using either a direct tool contact or a compliant intermediate layer. The following shall be cause for rejection (see Figure 2.10-38).

a. Evidence of separation or lack of adhesion. All beams must be bonded.

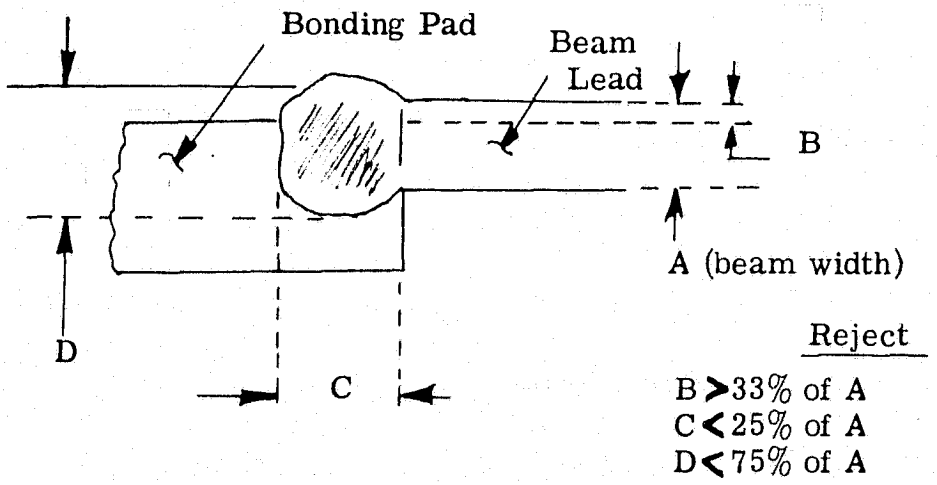
b. Cracks or tears in the bond area.

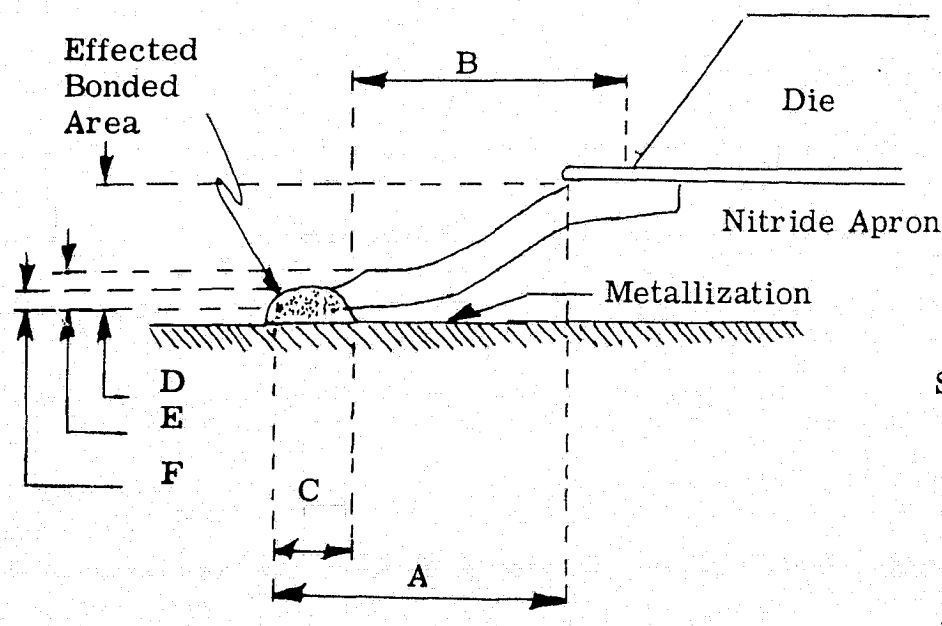
c. Voids that reduce the bond area by more than 33 percent.

d. Lack of compression indentations visible across the entire bond width.

e. Bond(s) with greater than 33 percent of the undeformed beam off of the bonding pad.

f. Compression indentation length less than 25 percent of the beam-lead width.





A - beam lead length
B - unbonded length
C - compression indention length
D - bugging height
E - undeformed beam thickness
F - deformed thickness

FIGURE 2.10-38

2.10.2.2.2.8 Internal Wires

The following shall be cause for rejection:

a. Any wire that touches another wire, package post, unglassivated operating metallization, die, or any portion of the package.

b. Excessive loop or sag in any wire such that it comes closer than four wire diameters to another wire, package post, unglassivated operating metallization, die, or portion of the package.

c. Nick(s), cut(s), crimp(s), scoring, or neckdown in any wire which reduces the wire diameter by more than 25 percent.

d. Missing wires.

e. Attached extra wires greater than two wire diameters in length at the bonding pad or four wire diameters in length at the package post.

f. Tearing at the junction of the wire and the bond.

g. Any wire that has no arc.

h. Wire crossing over another wire.

2.10.2.2.2.9 Package Condition

The following shall be cause for rejection:

a. Foreign material on the surface of the die, substrate, or within the package including the surface of the cover or cap.

b. Foreign material that bridges metallization paths, two package leads, lead to package metallization, or any combination thereof.

2.10.3 Summary

The following details shall be specified in the applicable procurement document:

a. Where applicable, any conflicts with approved circuit design topology or construction.

b. Where applicable, gages, drawings, and photographs which are to be used as standards for operator comparison.

c. Where applicable, specific magnification.

2.11 Design and Fabrication of a Typical Multilayer Circuit

The following is a brief description of the UHF Digital Frequency Synthesizer, a portion of which was selected for artwork generation and fabricated to test the guidelines and materials investigated during the initial phase of this program. This circuit is the sole property of ECI and its electrical design is to be considered company proprietary by all parties concerned.

ECI's Digital Frequency Synthesizer in its discrete form produces radio frequency signals in the range of 200 to 400 MHz, providing the L. O. (Local Oscillator) injection for the receiver and the exciting signal for the transmitter. The "synthesized" signal attains the frequency stability of a single stable crystal oscillator designed for communications equipment applications via a phase locked loop (PLL). The PLL compares the phase of the VCO and the reference signal and develops an error voltage to maintain phase lock. The block diagram of Figure 2.11-1 illustrates the critical components in the PLL. The programmable frequency divider provides the channelization required by varying the ratio of input to output frequency. A detailed block diagram of the divider or "N Counter" provides channel spacings to 25 kHz centers, 7000 channels across the UHF band.

Two additional functions are provided by the logic section proposed for this effort. The first is a simple arithmetic unit providing the addition or deletion of 70 MHz from the synthesizer frequency setting. This function is required in transceiver applications with a 70 MHz first IF. The second function illustrated is the FSK data generator. The synthesizer is automatically programmed to the selected channel. As FSK data is applied, the synthesizer is programmed up or down one data increment. For example, a Link 4 data system requires 25 kHz channel spacings and ±20 kHz FSK data.

The logic block proposed contains approximately 30 TTL packages, speeds range up to 50 MHz. Low power families such as 54L, 54 LS and CMOS were considered for this design.

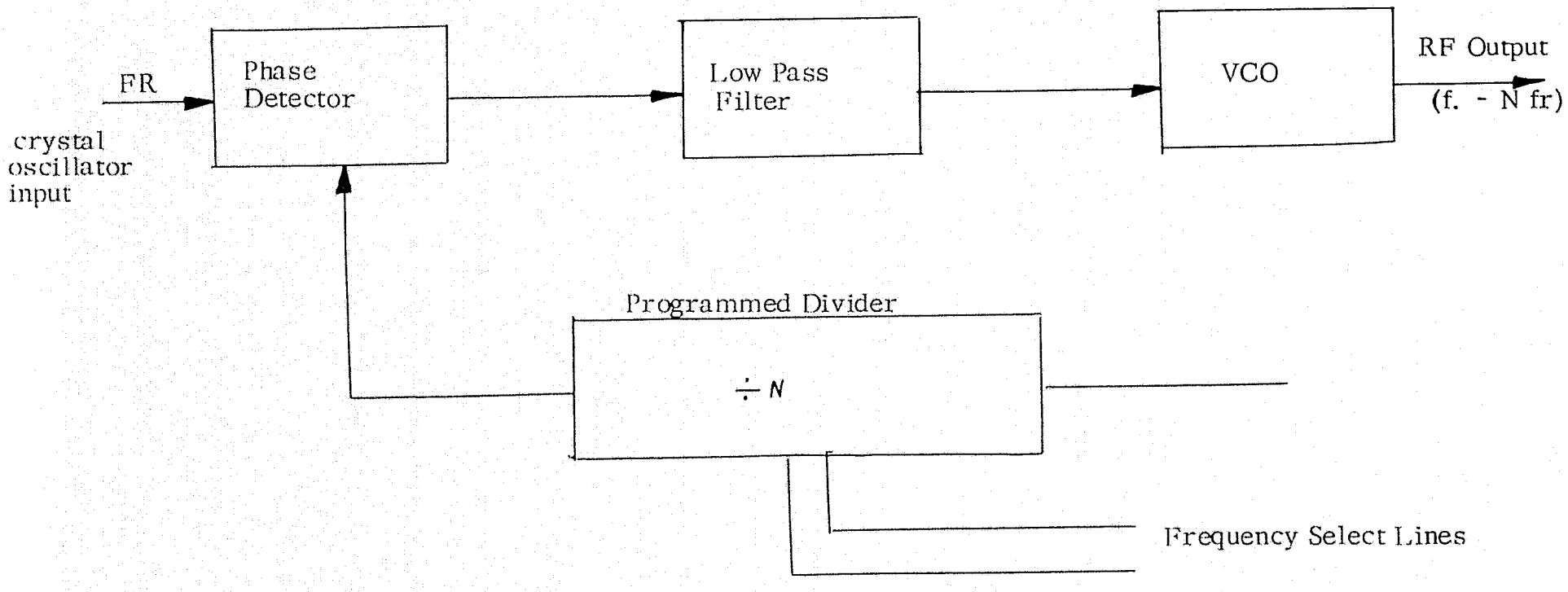


FIGURE 2.11-1. PHASE LOCKED LOOP

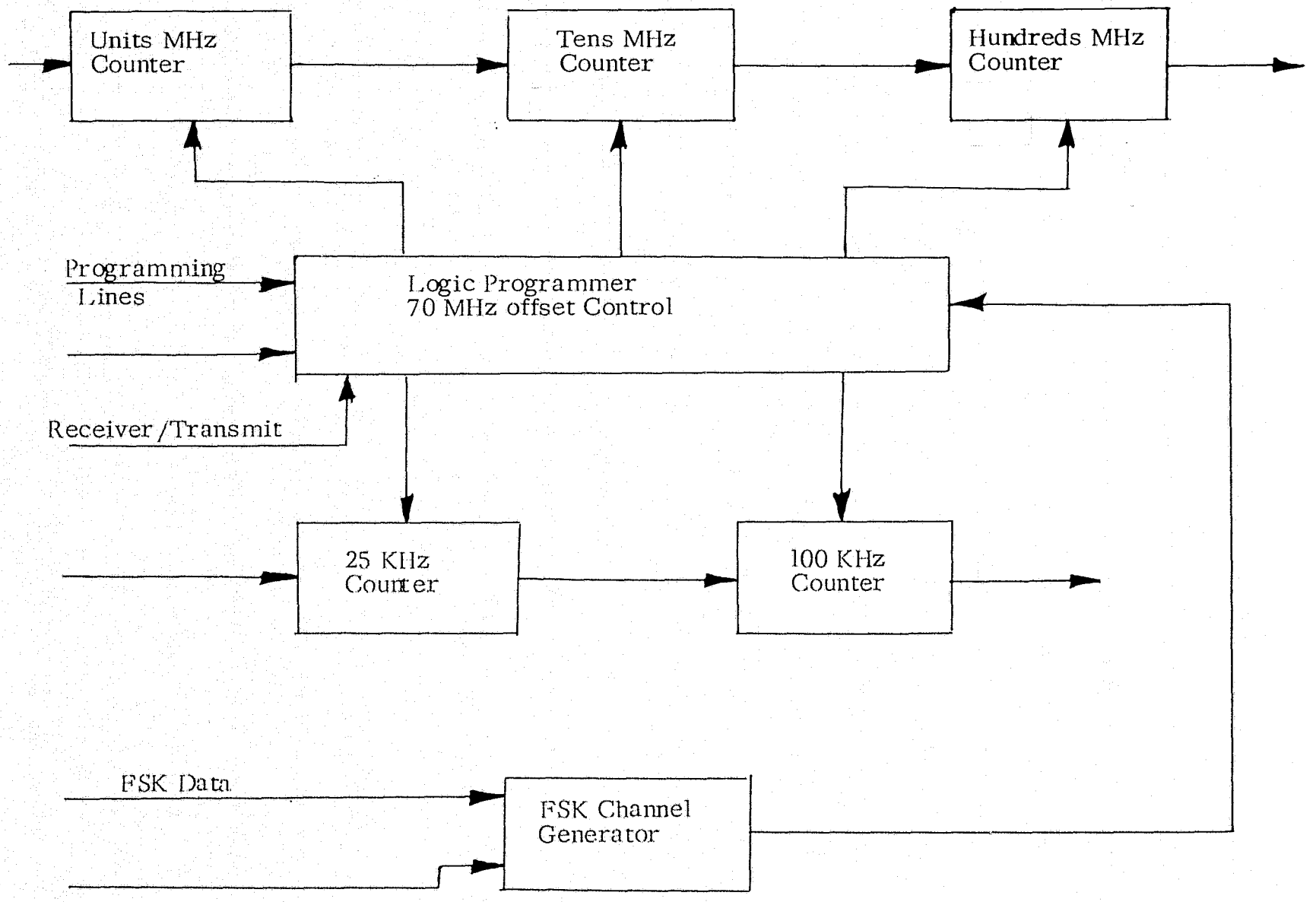

Units MHz Counter
Tens MHz Counter
Hundreds MHz Counter
Programming Lines
Logic Programmer 70 MHz offset Control
Receiver/Transmit
25 KHz Counter
100 KHz Counter
FSK Data
FSK Channel Generator

FIGURE 2.11-2

2.11.1 Components Procurement

Components for the synthesizer were ordered with a temporary hold up in layout caused by lack of component information sheets on some of the chip and beam lead devices. The following list of material was initially ordered.

Packaged Devices	Chip	Vendor	Quantity Ordered
CRI (5.6V)	IN752	Motorola	25
SN74S112Y	SN74S112Y	TI	50
SN5400J	MCBC5400	Motorola	31
SN5430J	MCBC5430	Motorola	38
SN5475J	MCC5479	Motorola	30
BL54LS196	BL54LS196Y	TI	100
BL54LS197	BL54LS197Y	TI	100
BL54LS20	BL54LS20Y	TI	100
SN5410J	MCBC5410	Motorola	31
BL54L04	BL54LS04	TI	100
SN5427J	MCC5427	Motorola	59
BL54L86	BL54L86Y	TI	100
BL54LS83	BL54LS83Y	TI	100
SN5403J	MCC5403	Motorola	61
SN5408J	MCC5408	Motorola	59
BL54L00Y	BL64L00Y	TI	100
SN54S64J	54S64	TI	50
SN54S112J	SN74S112Y	TI	50
Package IP1610	---	Isotronics	25

The engineering parts list was made after a commitment was received from the component vendors.

CIRCUIT NO. X-545 CIRCUIT TITLE PROGRAMMABLE THICK FILM ✓ THIN FILM ____

ENGINEER C. JACKSON DATE ____ DEPT. 640 REV ____ DATE ____ REV ____ DATE ____

DESIGNER P.C. HENNIGAN DATE 10-4-74 CHG. NO. 53226-640-03 REV ____ DATE ____ REV ____ DATE ____

PART	REF. DES.	VALUE OR TYPE	TOL	QTY.	VENDOR	VENDOR NO.	E.C.I. NO.	PART SIZE	REMARKS
IC	U13,20		–	2	MOT	MCBC5400			
"	U3,4		–	2	"	MCC5403			
"	U5		–	1	"	MCC5408			
"	U25		–	1	"	MCBC5410			
"	U9		–	1	"	MCC5427			
"	U23		–	1	"	MCBC5430			
"	U14,24		–	2	"	MCC5479			
"	U6		–	1	TI	BL54L00Y			
"	U7,10		–	2	"	BL54LS04			OR BL54L04
"	U18		–	1	"	BL54LS20Y			
"	U2,8		–	2	"	BL54LS86			OR BL54L86
"	U15,16,26		–	3	"	BL54LS196Y			
"	U17,21,22		–	3	"	BL54LS197Y			
"	U1		–	1	"	SN54LS83Y			
"	U11		–	1	"	SN74S64Y			OR 54S64
"	U12,13		–	2	"	SN74S112Y			
DIODE	CR1	5.6V		1	MOT	1N752			
PACKAGE					ISOTRONICS	IP1610			
INDUCTOR	L1	.15 UH							DEPOSITED

2-144

NOTES:

2.11.2 Layout Procedure

The rough engineering schematic was drawn and checked out by the responsible electrical engineer with notations made as to sensitive circuit areas. Special consideration was given to power requirements and potential "cross talk" areas. The rough schematic was redrawn incorporating the information required for layout and placed on format for later distribution.

Component "dolls" were drawn up to scale using vendor information sheets. The "dolls" were drawn to the maximum tolerance specified to prevent interference. The total component area required was calculated with interconnects considered using the following formula:

$CF_s = A$ Where C = Electrical connections

F_s = Space factor (.0043)

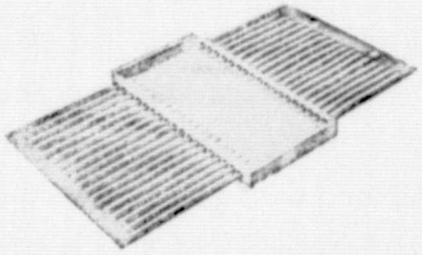
A = Area (in^2)

$A = 345$ (connections) $.0043$

$A = 1.5\ in^2$

This formula was imperically derived from a computer study of previous layouts performed at ECI. The schematic showed a need for 34 IP/OP connections with a request for additional test points if sufficient pin space was available.

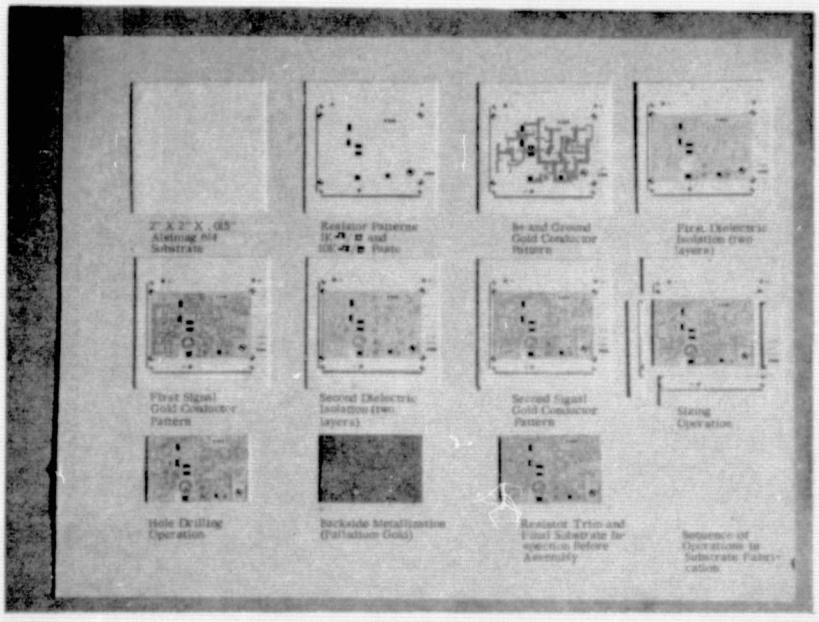
A search of vendor package sheets showed several package configurations with a substrate area of $1.5\ in^2$. Most of the package vendors contacted quoted 3 to 6 month deliveries and/or minimum quantities of 100 pieces. However, the Isotronics Corporation promised a rapid delivery for small quantities (25 in two weeks). The substrate area for the Isotronics IP1610 package is 1.5 inches x 1.0 inches. This package also has a desirable pin configuration with 32 leads on each of the long sides being standard. This package may be solder or weld sealed for environmental protection.

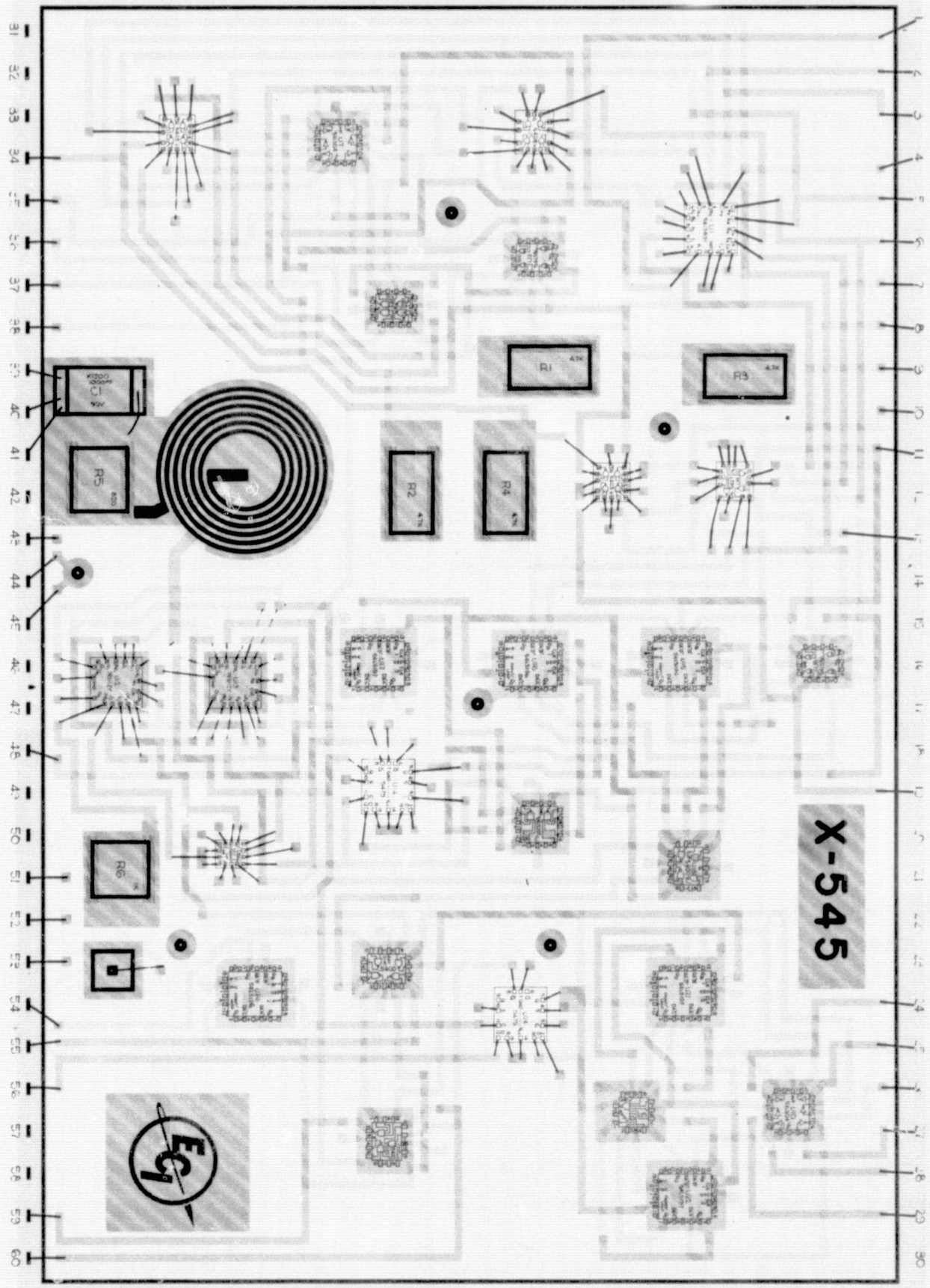


ISOTRONICS IP1610 PACKAGE

The doll layout was attempted at a scale of 20:1 with colored pencil interconnections. Several revisions were incorporated before the enclosed doll layout was considered acceptable. The circuit sensitivity required that the substrate backside be metallized as a ground plane and frontside ground "groupings" be connected by metallized through holes in the substrate.

The artwork was produced on a coordinatograph cut Rubylith system to a scale of 20:1 with an accuracy of ±.0005 in/48 inches. The completed artwork was reduced to 1:1 by photo reduction methods with the resultant silk screen positives delivered to the thick film laboratory for processing. The screens were fabricated and the thick film screen printing was carried out as shown in the following illustrations of the various steps required for multilayer fabrication.





2. 11. 3 Screen Fabrication

A total of seven screens were required to fabricate the thick film circuit. Resistor, dielectric and backside metallization screens were fabricated using 200 mesh stainless steel screen. The B+, ground plane, and two signal level screens were fabricated using 325 mesh stainless steel screen. All screen material was mounted to the frames at a 45^{O} angle with epoxy adhesive while stretched on a screen stretcher to assure proper screen tension.

The emulsion used was Azacol "R" with three coats applied by squeegee using a polyester backing as described in the Screen Fabrication section (2. 6. 1).

2. 11. 4 Thick Film Fabrication

The substrates processed were standard 2 inch X 2 inch X . 015 inch AlSiMag 614 substrates. As shown in the fabrication sequence (Figure 2. 11-5), the resistors were printed and fired at $900^{O}C$ to the appropriate profile. The next screening operation was that of the B+ and ground and resistor termination layer. The third screening operation consisted of screening and firing two layers of dielectric with visual inspection between each layer to verify open vias and absence of pinholes. The next screening operation was the first signal conductor level containing the spiral conductor. All conductor and dielectric layers were fired at $800^{O}C$ to the appropriate profile. After inspection of the first signal level, the second dielectric level was screened and fired in two layers. The second signal level was then screened and fired with a close optical inspection to verify overall circuit integrity.

The sizing operation was performed on a diamond scribing machine with backside scribing registered to the frontside alignment marks.

The hole drilling operation was performed with an optically aligned air abrasive pulse jet. The backside metallization was applied by screen printing and optically inspected to ensure penetration of the metallization through the holes to the frontside metallization.

After the thick film fabrication steps were completed, the substrates were optically inspected and electrically probed to assure circuit interconnect compliance and absence of physical defects.

A lot of ten thick film circuits were submitted to Quality Control inspection for approval prior to submitting them to electrical and mechanical tests.

2. 11. 5 Electrical and Mechanical Test

A set of 39 test points was established for continuity and shorts probing before and after thermal shock. It has been found that severe thermal shock

(+125°C to -55°C, five cycles) is a very useful test for determining structural and electrical integrity of thick film circuits. The 39 test points were chosen to provide resistance measurements on both resistors and long fine line conductor traces. The test points also incorporated maximum crossovers to determine shorts occurrence.

2.11.6 Test Results

The thick film circuits were electrically probed for resistance and shorts measurements prior to and after thermal shock. A Hewlett-Packard 3440A digital voltmeter with a 3444A D. C. multi-function unit was used for resistance measurements and a Hickok Model DP200 digital capacitance read out was used for shorts measurements.

The following is a set of representative resistance readings taken before and after five cycles of thermal shock from -55°C to +125°C:

(Sample Number MLB 2)
Resistivity and Continuity

From	To	Before T. S.(Ω)	After T. S. (Ω)
TP1	TP2	0.6	0.6
TP1	TP3	0.7	0.6
TP4	TP5	0.5	0.5
TP6	TP7	0.5	0.5
TY6	TP8	0.3	0.3
TP6	TP9	0.3	0.3
TP10	TP11	0.4	0.4
TP10	TP12	0.6	0.5
TP10	TP13	0.4	0.3
TP14	TP15	0.8	0.7
TP14	TP16	0.8	0.7
TP17	TP18	0.7	0.6
TP17	TP19	0.6	0.5
TP17	TP20	0.4	0.4
TP21	TP22	0.4	0.3
TP21	TP23	0.4	0.3
TP21	TP24	0.6	0.5
TP25	TP26	0.4	0.3
TP25	TP27	0.4	0.4

	From	To	Before T. S. (Ω)	After T. S. (Ω)
(Grd)	TP28	TP29	0.3	0.3
	TP28	TP30	0.3	0.3
	TP28	TP31	0.3	0.3
	TP28	TP32	0.3	0.3
	TP28	TP33	0.3	0.3
(B+)	TP34	TP35	0.1	0.1
	TP34	TP36	0.1	0.1
	R1	-	4714	4713
	R2	-	4716	4716
	R3	-	4716	4718
	R4	-	4713	4715
	R5	-	822	821
	R6	-	1003	1001
(Coil)	TP37	TP38	4.6	4.3

Shorts Occurrance

	From	To	Before T. S.	After T. S.
(B+)	TP34	TP1	Open	Open
	TP34	TP2	Open	Open
	TP34	TP3	Open	Open
	TP34	TP4	Open	Open
	TP34	TP5	Open	Open
	TP34	TP6	Open	Open
	TP34	TP7	Open	Open
	TP34	TP8	Open	Open
	TP34	TP9	Open	Open
	TP34	TP10	Open	Open
	TP34	TP11	Open	Open
	TP34	TP12	Open	Open
	TP34	TP13	Open	Open
	TP34	TP14	Open	Open
	TP34	TP15	Open	Open
	TP34	TY16	Open	Open
	TP34	TP17	Open	Open
	TP34	TP18	Open	Open
	TP34	TP19	Open	Open

	From	To	Before T. S.	After T. S.
	TP34	TP20	Open	Open
	TP34	TP21	Open	Open
	TP34	TP22	Open	Open
	TP34	TP23	Open	Open
	TP34	TP24	Open	Open
	TP34	TP25	Open	Open
	TP34	TP26	Open	Open
	TP34	TP27	Open	Open
	TP34	TP28	Open	Open
(Grd)	TP28	TP1	Open	Open
	TP28	TP2	Open	Open
	TP28	TP3	Open	Open
	TP28	TP4	Open	Open
	TP28	TP5	Open	Open
	TP28	TP6	Open	Open
	TP28	TP7	Open	Open
	TP28	TP8	Open	Open
	TP28	TP9	Open	Open
	TP28	TP10	Open	Open
	TP28	TP11	Open	Open
	TP28	TP12	Open	Open
	TP28	TP13	Open	Open
	TP28	TP14	Open	Open
	TP28	TP15	Open	Open
	TP28	TP16	Open	Open
	TP28	TP17	Open	Open
	TP28	TP18	Open	Open
	TP28	TP19	Open	Open
	TP28	TP20	Open	Open
	TP28	TP21	Open	Open
	TP28	TP22	Open	Open
	TP28	TP23	Open	Open
	TP28	TP24	Open	Open
	TP28	TP25	Open	Open
	TP28	TP26	Open	Open
	TP28	TP27	Open	Open

From	To	Before T.S.	After T.S.
TP21	TP25	Open	Open
TP21	TP14	Open	Open
TP6	TP10	Open	Open
TP1	TP4	Open	Open
TP1	TP6	Open	Open

2.11.6.1 Test Result Conclusions

The test results showed a very stable interconnect metallization system and dielectric isolation. None of the samples tested developed opens or shorts and the deviation of the resistance readings were well within the read out tolerances. Very little difference was noted from sample-to-sample on readings from the same test points. This is a fairly accurate method of determining repeatability of processes.

2.11.7 Test Circuit Final Assembly

At this writing, component delivery has not been completed. The final circuit assembly and test results will be published as an addendum to the NASA COR for distribution at the discretion of the NASA distribution center.

2.12 Materials Evaluation Study

A materials evaluation study was undertaken at ECI as part of NASA contract NAS8-29624. A list of conductor and/or dielectric paste manufacturers was compiled and their representatives notified by letter of the intended evaluation program.

The purpose of the evaluation program was to determine applicability of existing thick film compositions to fine line multilayer fabrication. The paste manufacturers were advised that the materials to be evaluated must be commercially available off-the-shelf compositions and not specifically formulated for this evaluation. The evaluation program was intended to investigate materials in relation to the following characterizations:

1. Screen printing characteristics
2. Fine line conductor definition
3. Dielectric via definition
4. Conductor continuity and resistivity
5. Dielectric pinholing and shorts potential
6. Interreaction between conductor and dielectric compositions

The test pattern illustrated in Figure 2.8-5 (Test Pattern Utilization section 2.8) was used for the conductor and dielectric materials evaluation.

The following list of manufacturers agreed to participate in the program and furnish conductor and/or dielectric materials.

Manufacturer	Code	Material	Firing Atmosphere
Thick Film Systems	1C	Gold Conductor Vitr-Au-Less 4007 Fine Line	Air
	2C	Gold Conductor 3009	Air
	1SC	Copper Conductor EX513 (results to be confidential)	N2
	1D	Dielectric - ISO-OHM 1017 RCA	Air

Manufacturer	Code	Material	Firing Atmosphere
	2D	Dielectric - ISO-OHM 1005 TCG	Air
	11D	Dielectric - ISO-OHM 1017 RCY	Air
Engelhard	3C	Gold Conductor - Fine Line A-2894	Air
	4C	Gold Conductor - Molecular Bonding A-2789	Air
	5C	Gold Conductor - Squeege Gold A-1560	Air
	2SC	Nickel Conductor - Molecular Bonding A-2884	Air
	3SC	Aluminum Conductor - Molecular Bonding A-2746	Air
	3D	Dielectric - Zero flow A-2835	Air
DuPont	6C	Gold Conductor - Fine Line 9260	Air
	7C	Gold Conductor - Fine Line 8237	Air
	11C	Platinum Gold Conductor Fine Line 8653	Air
	4D	Dielectric 8299	Air
	5D	Dielectric 9429	Air
Electro Science	8C	Gold Conductor - Fine Line 8835-1B	Air
	9C	Gold Conductor - Fine Line 8835	Air
	*4SC	Nickel Conductor - Nickel 2502 H_2	H_2
	6D	Dielectric - 6408C	Air
	7D	Dielectric - 6408 CFB-M2	Air

Manufacturer	Code	Material	Firing Atmosphere
Cermalloy	*5SC	Copper Conductor - 7029	N_2
	*6SC	Nickel Conductor - 7028	N_2
EMCA	10C	Gold Conductor - Fine Line EXK3264	Air
	12C	Platinum Gold Conductor EXK3283	Air
	*7SC	Nickel Conductor - N16500	N_2
	8D	Dielectric - 3186B	Air
	9D	Dielectric - 3186C	Air
	10D	Dielectric - EXK3274	Air
Electro Oxide Corp.	12D	Dielectric - 6208	Air
	14C	Gold Conductor - 6990	Air
Sel-Rex Company	13C	Gold Conductor - DX-799	Air

* Special atmosphere required

2.12.1 Dielectric Compositions

The dielectric compositions were processed to the manufacturers recommended procedures using ECI laboratory and processing equipment. The dielectric test pattern screen was fabricated per the procedures described in the Screen Fabrication section (2.6.1), using 200 mesh stainless steel screen.

Four sample modes were established for evaluation of dielectric compositions (1) single layer - not fired, (2) single layer - fired, (3) double layer - not fired, (4) double layer - fired.

Capacitance measurements were made on multiple samples and averaged to give average capacitance per square inch. The samples used for capacitance measurements were double layers of fired dielectric with 8237 gold top and bottom plates.

Samples were randomly selected from each lot for optical inspection and photographic records. The following is a brief summation of the results of the screen and fire dielectric evaluation.

2.12.1.1 Thick Film Systems ISO-OHM 1017 RCA (1D)

Figures 2.12-1, 2.12-2, 2.12-3, and 2.12-4

The material was easily screened and clean-up with toluene solvent was easily accomplished. The unfired dielectric material had a relatively smooth appearance with a pale blue color. The fired dielectrics exhibited the typical ceramic appearance of this type dielectric with the retention of the blue coloration.

Definition on one layer fired was excellent with .006 inch square vias readily accomplished. Two layers of fired dielectric exhibited a lesser definition due to intrusion of material from the second screening. A definition of .008 inch square vias is practical with two layers fired. The average capacitance measured was 2400 pf/inch^2.

2.12.1.2 Thick Film Systems ISO-OHM 1005 TCG (2D)

Figures 2.12-5, 2.12-6, 2.12-7, and 2.12-8

The dielectric material, 2D, was similar to 1D in its screen printing characteristics. The unfired dielectric had a green coloration which helped in screen alignment Definition of one layer of fired dielectric was very good with .006 inch square vias possible. Two layers of fired dielectric allowed a definition of .008 inch. The surface of the dielectric in the two layers fired was somewhat coarse but no through pinholes were observed. The average capacitance measured was 2650 pf/inch^2.

2.12.1.3 Engelhard Zero Flow A-2835 (3D)

Figures 2.12-9, 2.12-10 2.12-11 and 2.12-12

The screen printed unfired dielectric dried quite well on the average with good healing of screen impressions. The coloration of both fired and unfired material was a dull green. Fired dielectric definition observed was .006 inch for single layer and .006 inch for double layer. Some slight reaction between the base metallization was observed but was attributed to solvent outgasing during firing. The bubbling of the dielectric resulted in a disturbance of the surface topography and some pinholing. The average capacitance observed was 2250 pf/in^2.

2 12.1.4 DuPont 8299 (4D)

Figures 2.12-13, 2.12-14, 2.12-15 and 2.12-16

Screen printing characteristics of this material were fair with wash-out easily accomplished using toluene. Definition on fired films was not quite as good as would be expected for this type dielectric. Single layer fired dielectric allowed .006 inch vias but double layering reduced the definition down to .010 inch. The fired films had a fairly smooth surface texture but pinholes could present a problem. The average capacitance observed was 3400 $pf/inch^2$.

2.12.1.5 DuPont 9429 (5D)

Figures 2.12-17, 2.12-18, 2.12-19, and 2.12-20

This dielectric material had a coral colored dye which burned out upon furnace firing. The fired dielectric was white in color and had a relatively smooth surface. No through pinholes were observed. Screen printing characteristics were excellent with clean-up easily accomplished using toluene. The fired dielectric definition was .004 inch for single layers and .008 inch for double layers. The average capacitance observed was 2750 $pf/inch^2$.

2.12.1.6 Electro Science 4608C (6D)

Figures 2.12-21, 2.12-22, 2.12-23 and 2.12-24

The unfired dielectric contained a dark blue pigmentation which burned out

during furnace firing. The paste residue left on the screen was difficult to wash out with toluene. The dielectric paste had a tendency to bubble during drying resulting in a porous surface topography after furnace firing. Definition was excellent for both single layer and double layer fired dielectrics. Single layer definition was .004 inch and double layer was .006 inch. The average capacitance for two layers of fired dielectric was 2750 pf/inch^2.

2.12.1.7 Electro Science 4608 CFB-M2 (7D)

Figures 2.12-25, 2.12-26, 2.12-27 and 2.12-28

The unfired dielectric material contained a dark blue pigment which burned out during furnace firing. The pigment was difficult to wash out of the screen. The fired dielectric was white to pale yellow and somewhat porous. Single layer via definition was .004 inch with double layer definition of .006 inch. Excessive bubbling during drying was observed resulting in a disturbed topography. A longer settling prior to a slow drying may help alleviate this problem. The average capacitance for this dielectric (2 layers) was 3500 pf/inch^2.

2.12.1.8 EMCA 3186B (8D)

Figures 2.12-29, 2.12-30, 2.12-31, 2.12-32

The unfired dielectric paste was of a pale blue coloration with single layer fired material close to clear in color. Double layers of fired dielectric were opaque white in color and somewhat coarse in texture. The via definition observed was .006 inch for single layer fired and .010 inch for double layer fired. Some pinholing was observed. The average capacitance measured was 3000 pf/inch^2.

2.12.1.9 EMCA 3186C (9D)

Figures 2.12-33, 2.12-34, 2.12-35, and 2.12-36

The screened unfired dielectric was pale blue in color and upon firing became almost transparent. The fired dielectric via resolution observed was .006 inch for single layer and .010 inch for double layers. This dielectric in double layered fired configuration was relatively pinhole free. The average capacitance measured was 3000 pf/inch^2

2.12.1.10 EMCA EXK3274 (10D)

Figures 2.12-37, 2.12-38, 2.12-39 and 2.12-40

The unfired dielectric had a blue pigmentation similar to 3186B and C materials. The color was burned out when the dielectric was fired leaving a translucent to white material. The fired dielectric was relatively pinhole free with via resolution of .008 inch for single layer and .010 inch for double layers of dielectric. The average measured capacitance was 2000 pf/inch^2.

2.12.1.11 Thick Film Systems 1017 RCY (11D)

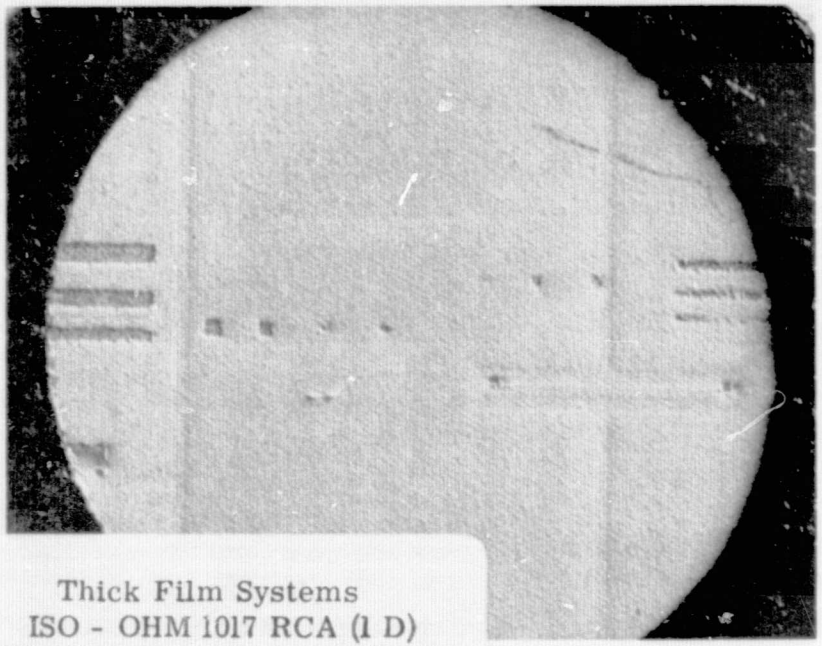
Figures 2.12-41, 2.12-42, 2.12-43, 2.12-44

The unfired dielectric material had a yellow pigmentation which burned out during furnace firing to leave a relatively smooth pinhole free dielectric with coloration from dull translucent to pale yellow for double layers of dielectric. The via definition observed was .004 inch for single layer fired and .008 inch for double layers fired. The average capacitance measured was 2250 pf/inch^2.

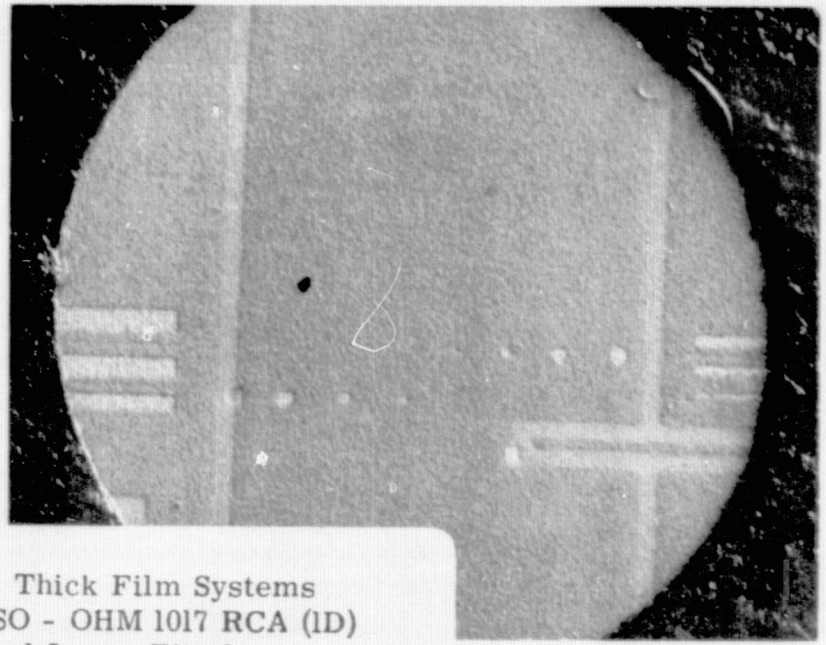
2.12-1.12 Electro Oxide Corporation 6208 (12D)

Figures 2.12-45, 2.12-46, 2.12-47, and 2.12-48

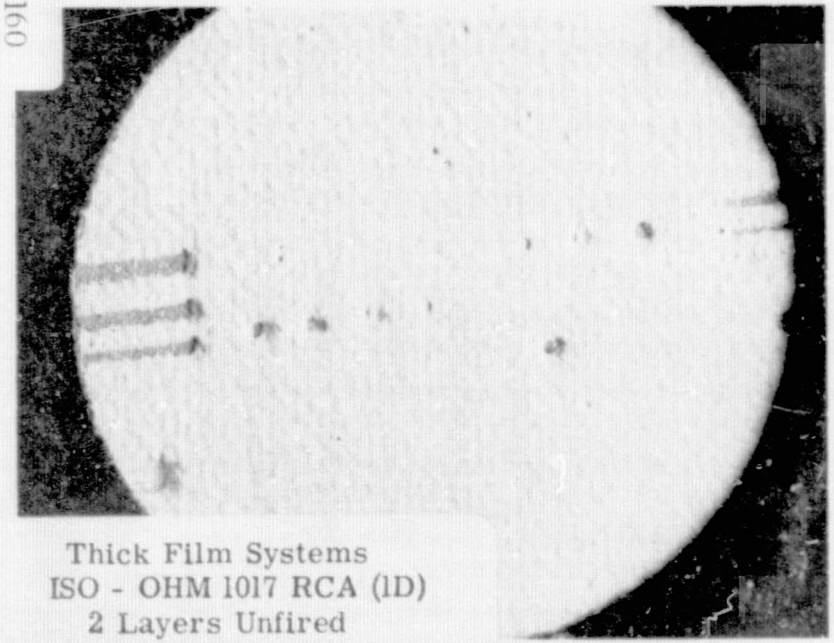
The unfired dielectric material was coarse in texture and white in color. Difficulty in screening was observed due to material drying rapidly and pulling from the substrate. The fired dielectric was glassy in appearance and via definition was .006 inch for both single and double screened dielectrics. The average capacitance measured was 2500 pf/inch^2.



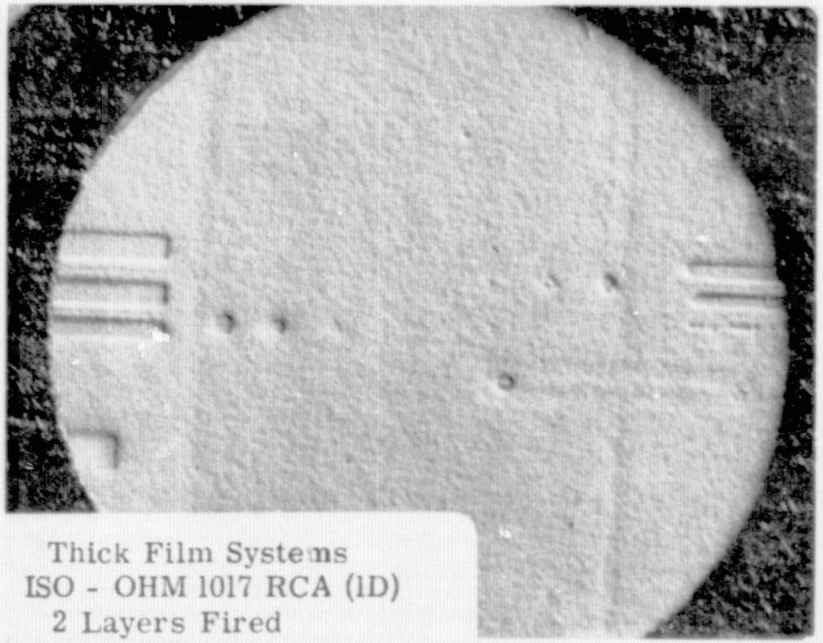
Thick Film Systems
ISO - OHM 1017 RCA (1 D)
1 Layer Unfired
FIGURE 2.12-1



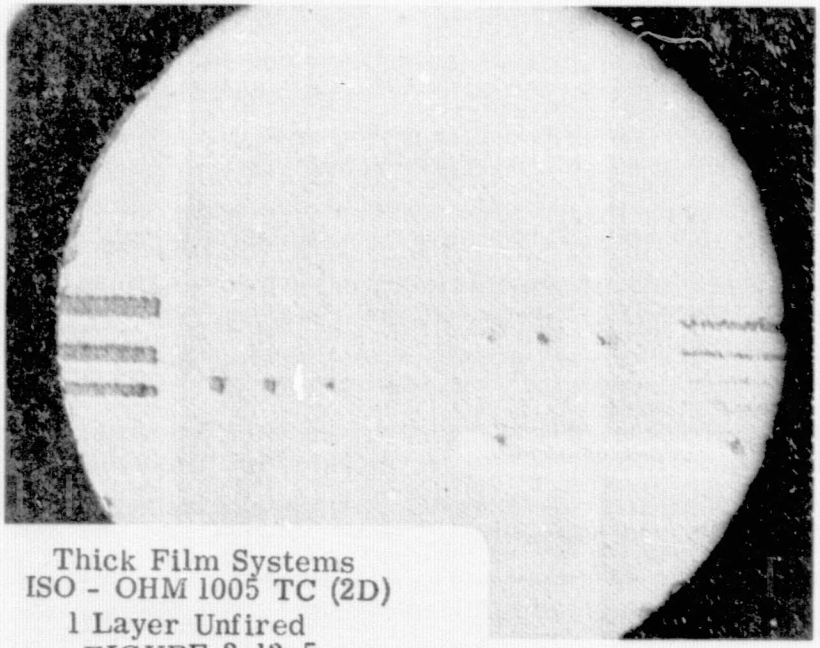
Thick Film Systems
ISO - OHM 1017 RCA (1D)
1 Layer Fired
FIGURE 2.12-2



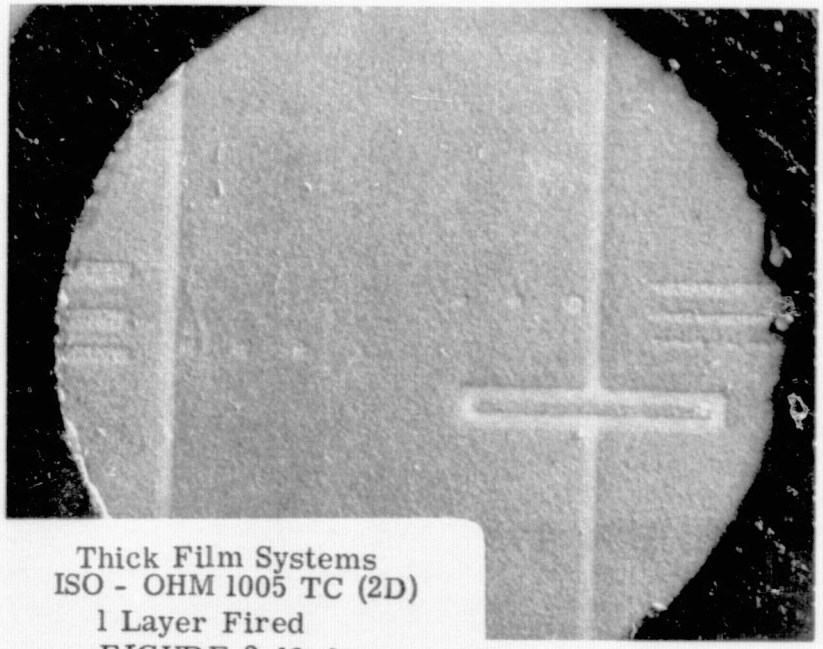
Thick Film Systems
ISO - OHM 1017 RCA (1D)
2 Layers Unfired
FIGURE 2.12-3



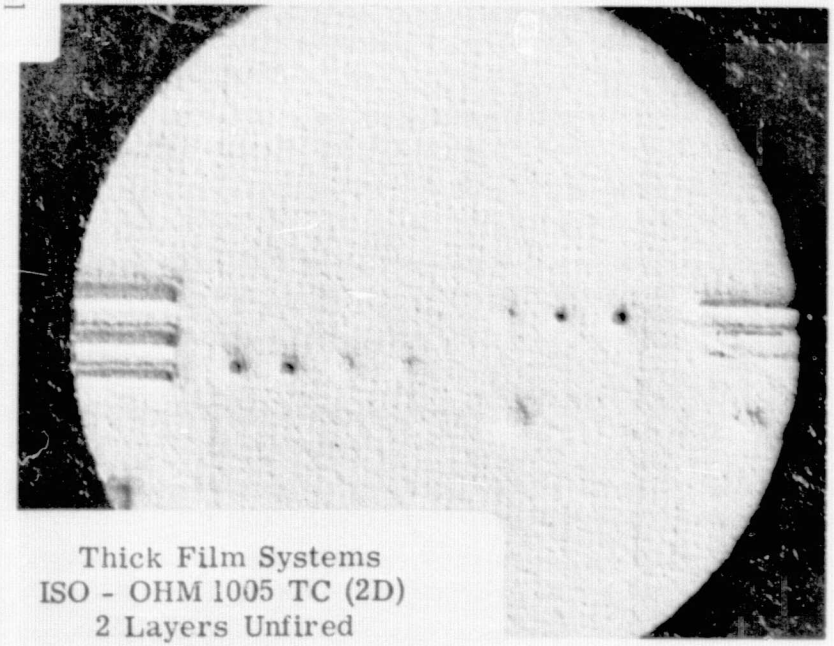
Thick Film Systems
ISO - OHM 1017 RCA (1D)
2 Layers Fired
FIGURE 2.12-4



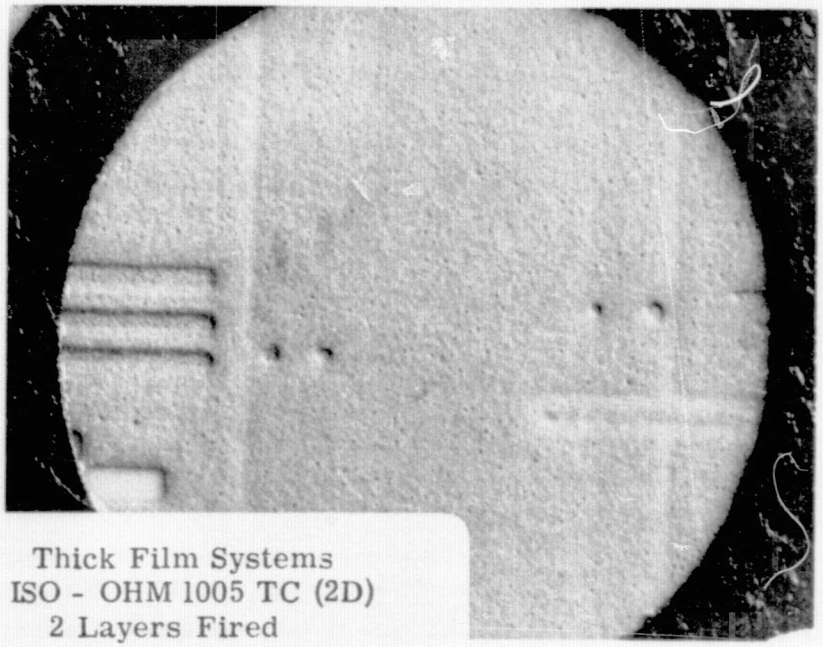
Thick Film Systems
ISO - OHM 1005 TC (2D)
1 Layer Unfired
FIGURE 2.12-5



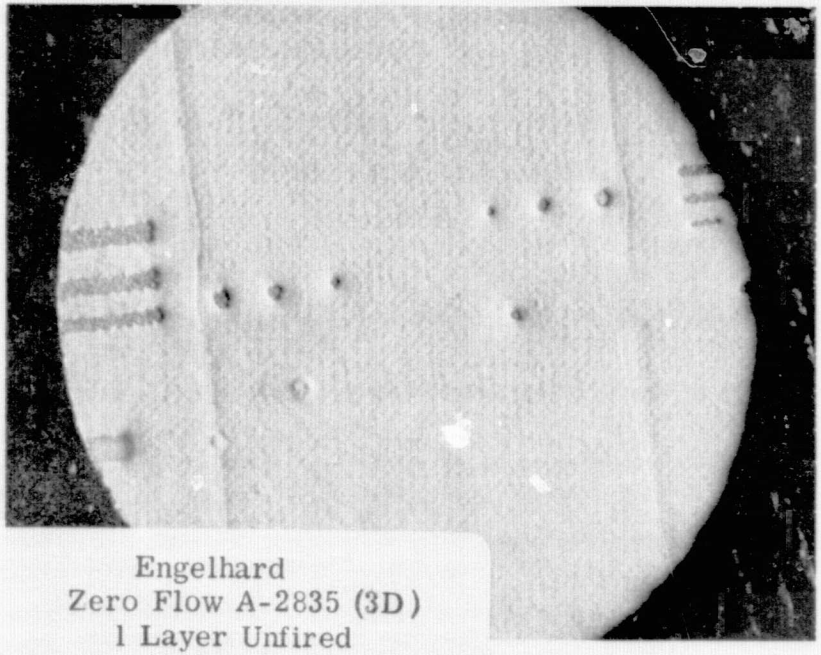
Thick Film Systems
ISO - OHM 1005 TC (2D)
1 Layer Fired
FIGURE 2.12-6



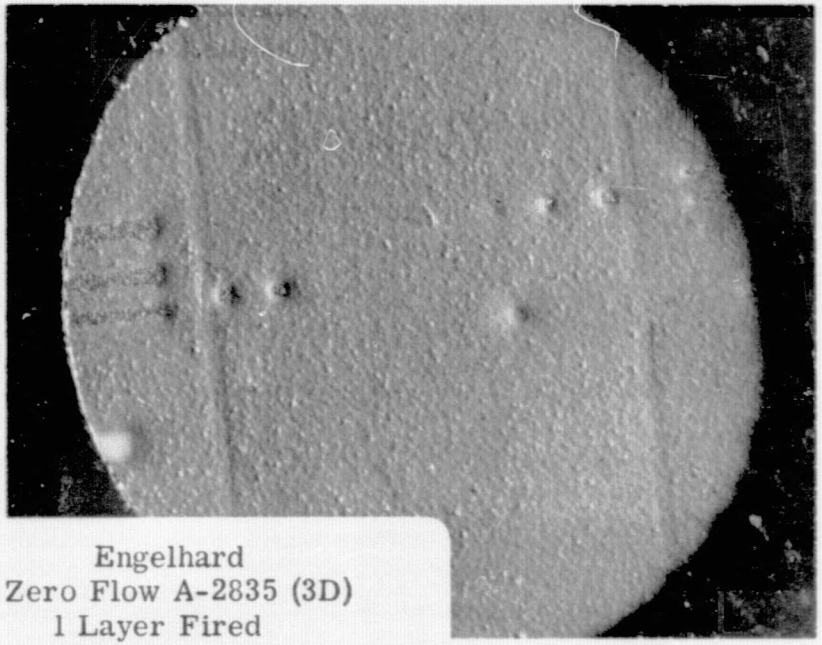
Thick Film Systems
ISO - OHM 1005 TC (2D)
2 Layers Unfired
FIGURE 2.12-7



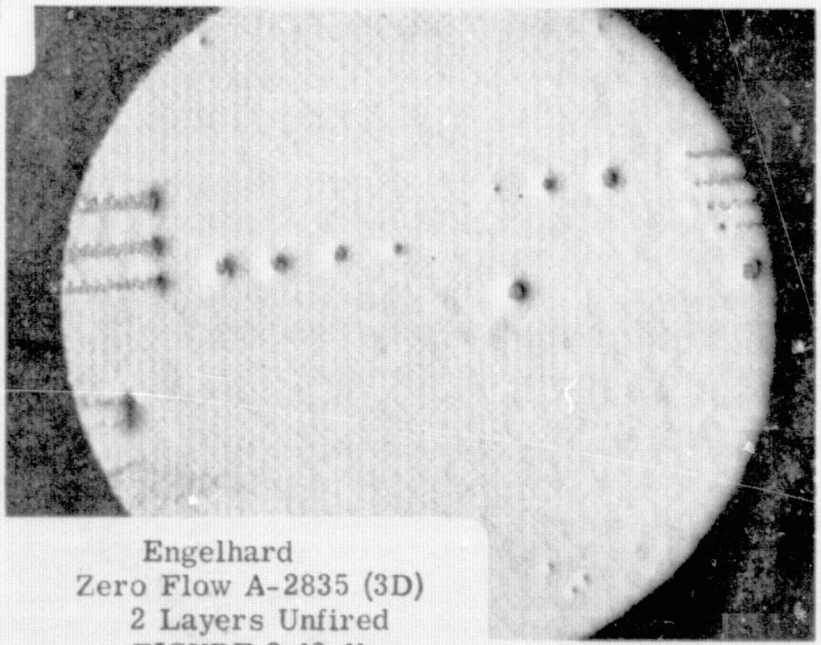
Thick Film Systems
ISO - OHM 1005 TC (2D)
2 Layers Fired
FIGURE 2.12-8



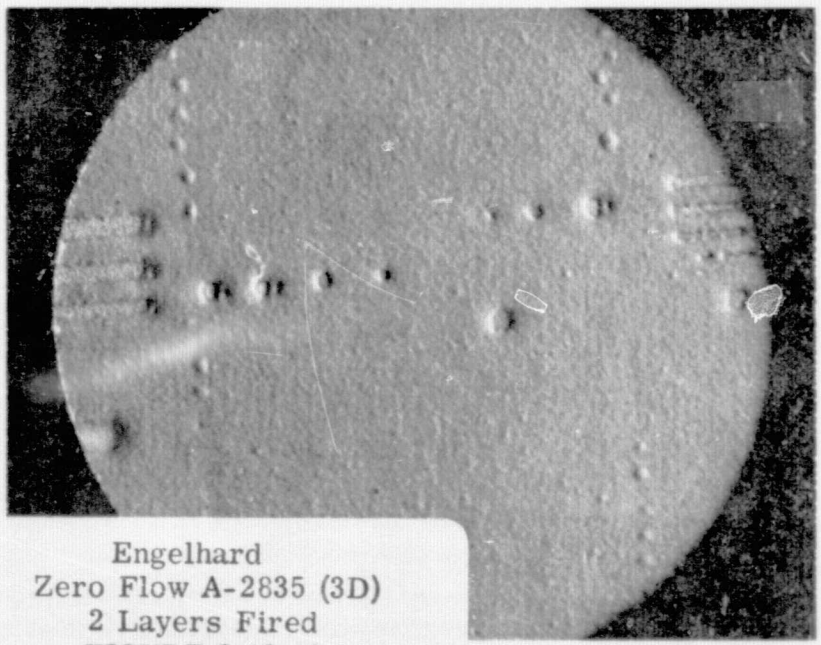
Engelhard
Zero Flow A-2835 (3D)
1 Layer Unfired
FIGURE 2.12-9



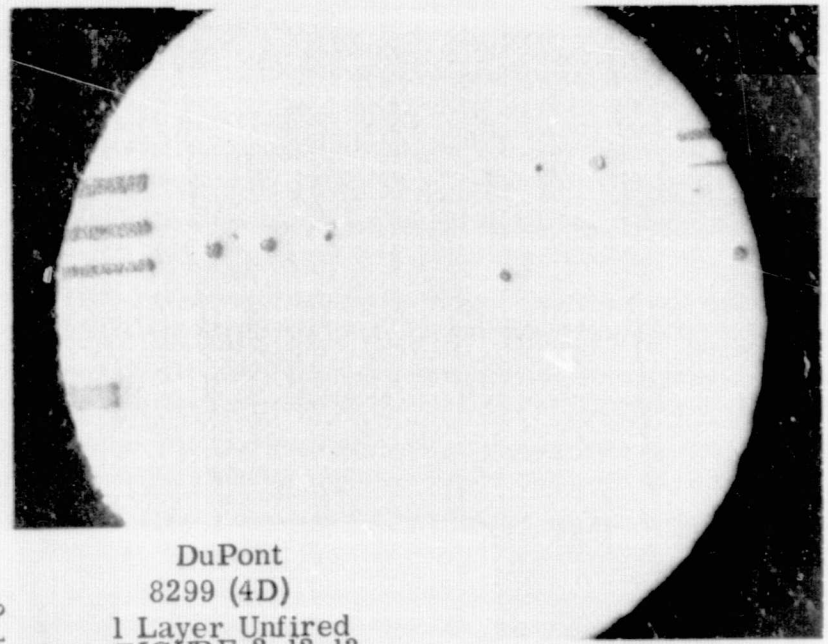
Engelhard
Zero Flow A-2835 (3D)
1 Layer Fired
FIGURE 1.12-10



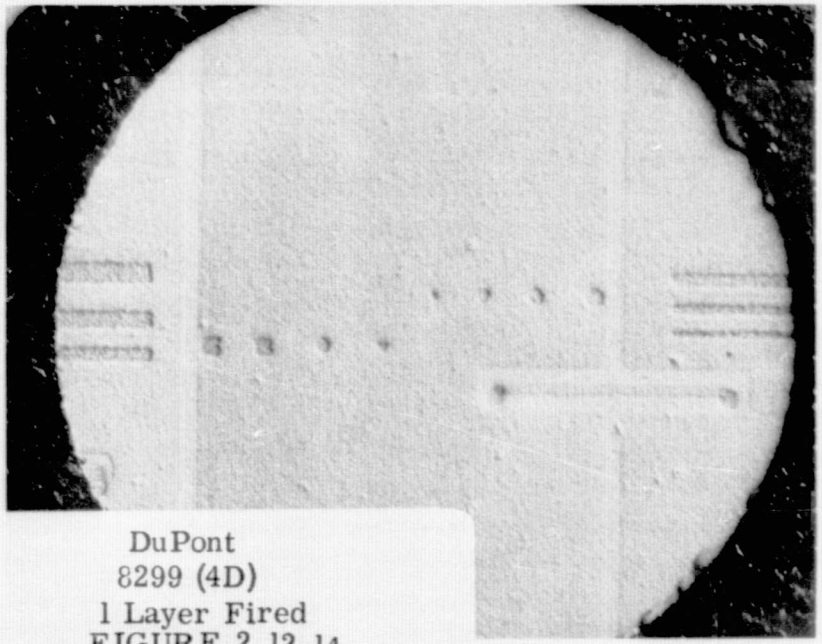
Engelhard
Zero Flow A-2835 (3D)
2 Layers Unfired
FIGURE 2.12-11



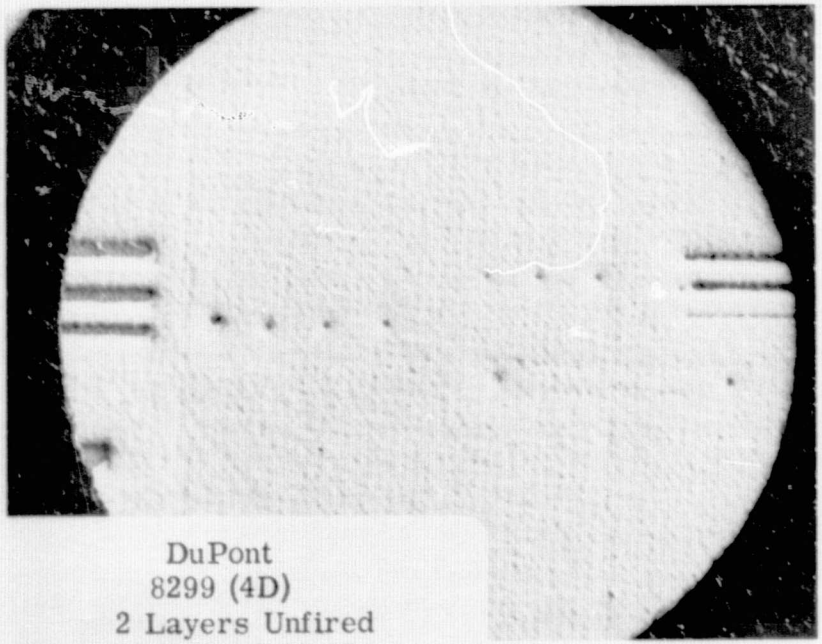
Engelhard
Zero Flow A-2835 (3D)
2 Layers Fired
FIGURE 2.12-12



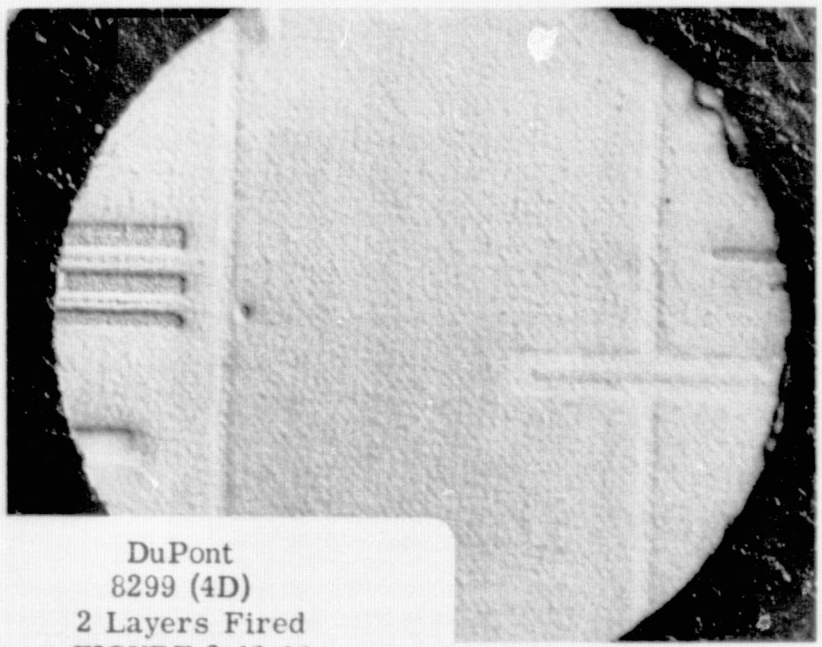
DuPont
8299 (4D)
1 Layer Unfired
FIGURE 2.12-13



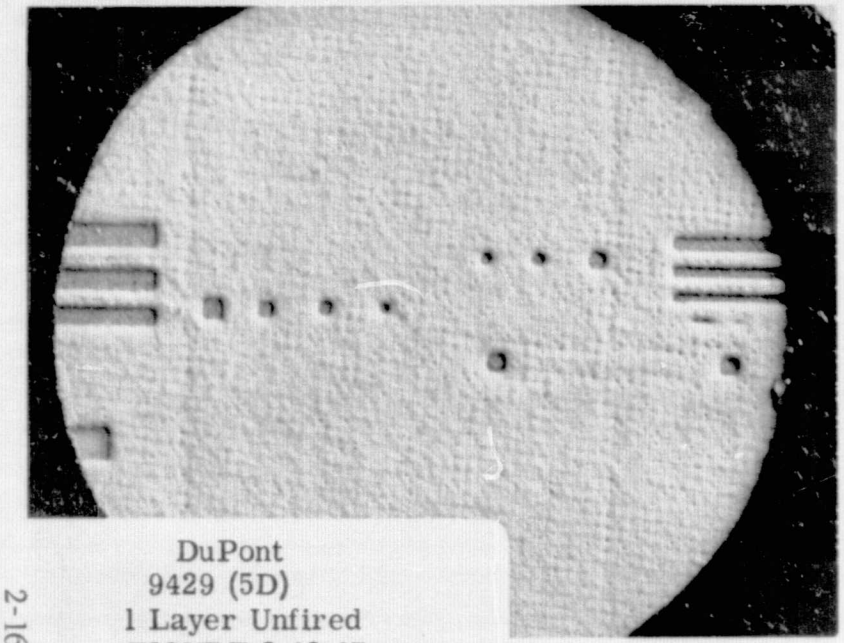
DuPont
8299 (4D)
1 Layer Fired
FIGURE 2.12-14



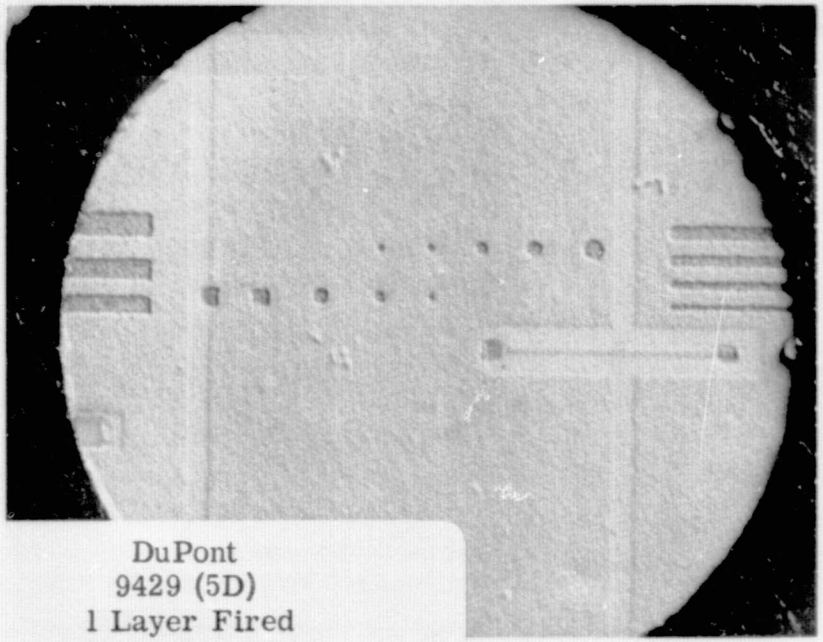
DuPont
8299 (4D)
2 Layers Unfired
FIGURE 2.12-15



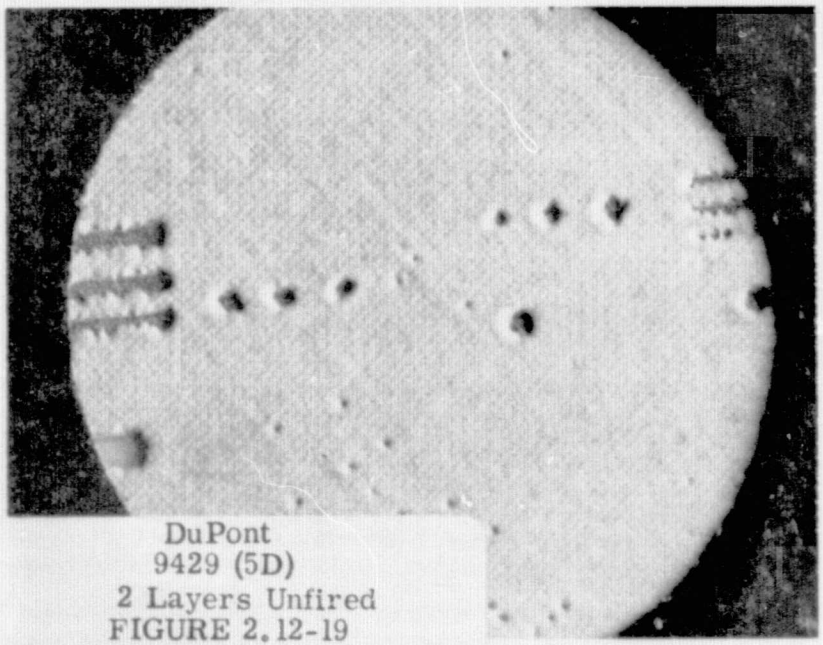
DuPont
8299 (4D)
2 Layers Fired
FIGURE 2.12-16



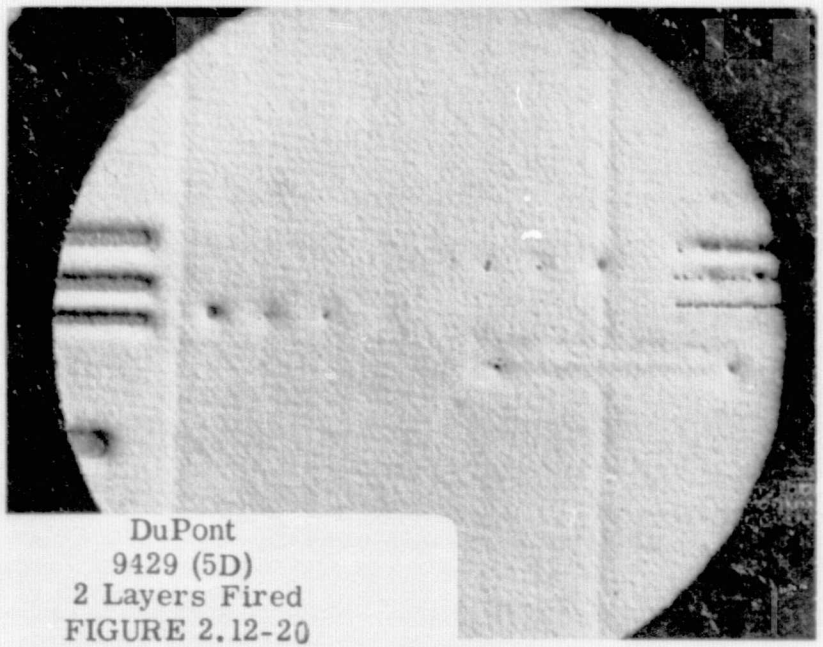
DuPont
9429 (5D)
1 Layer Unfired
FIGURE 2.12-17



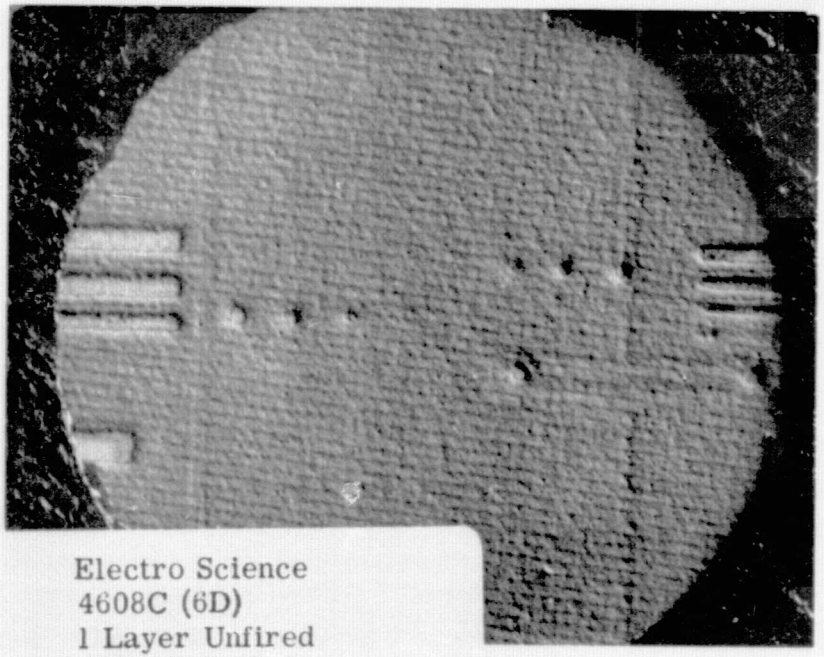
DuPont
9429 (5D)
1 Layer Fired
FIGURE 2.12.18



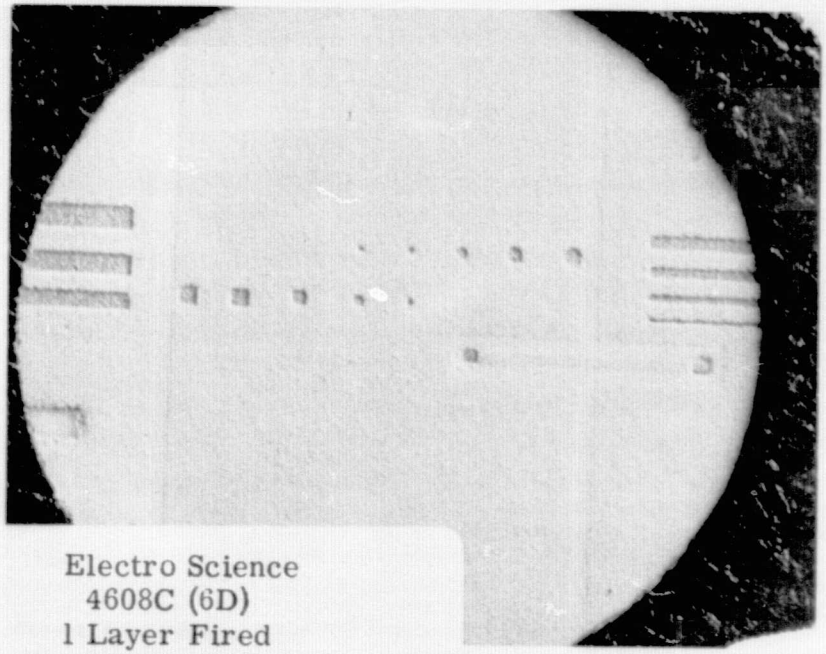
DuPont
9429 (5D)
2 Layers Unfired
FIGURE 2.12-19



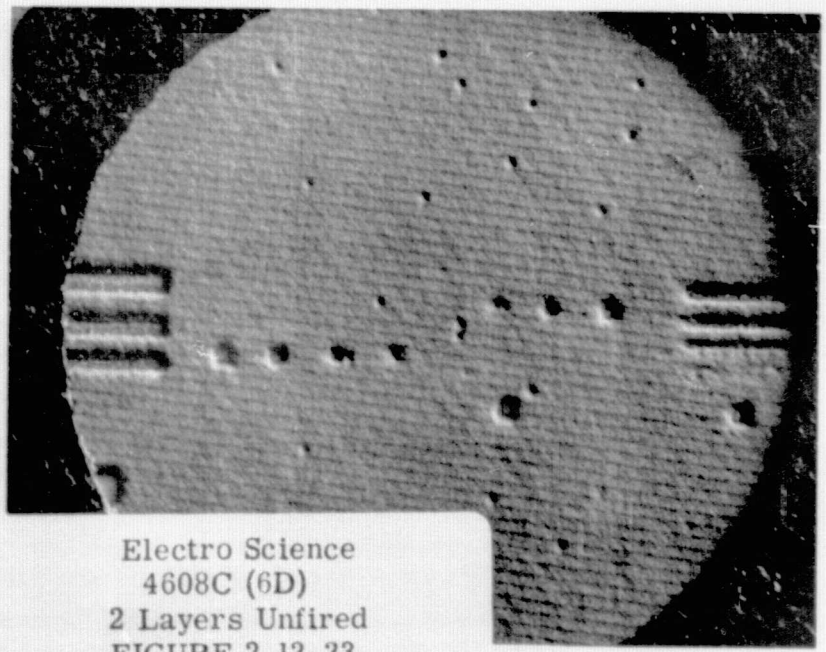
DuPont
9429 (5D)
2 Layers Fired
FIGURE 2.12-20



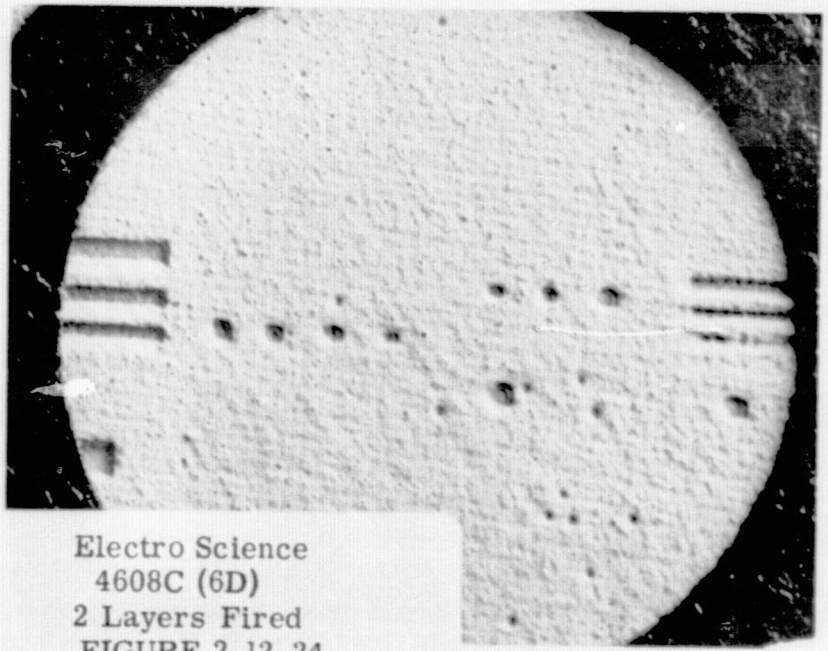
Electro Science
4608C (6D)
1 Layer Unfired
FIGURE 2.12-21



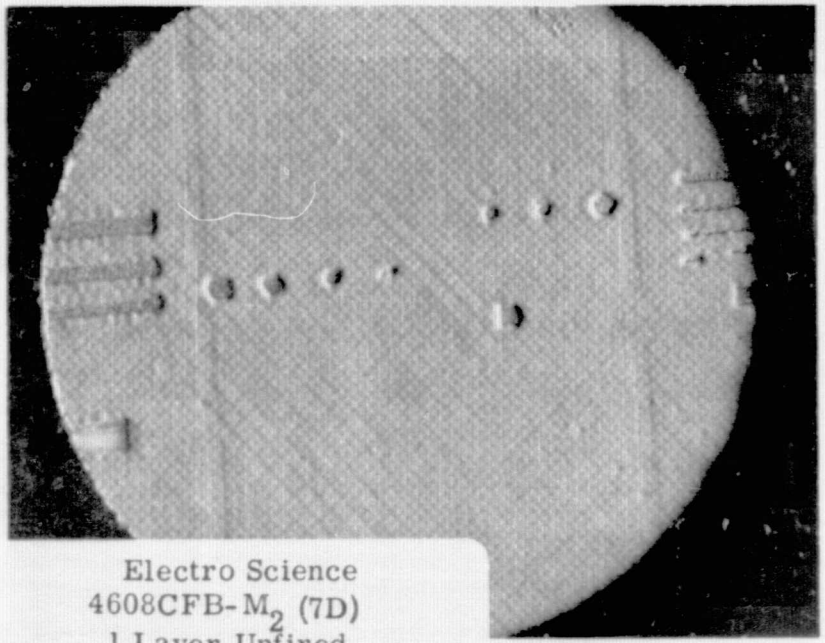
Electro Science
4608C (6D)
1 Layer Fired
FIGURE 2.12-22



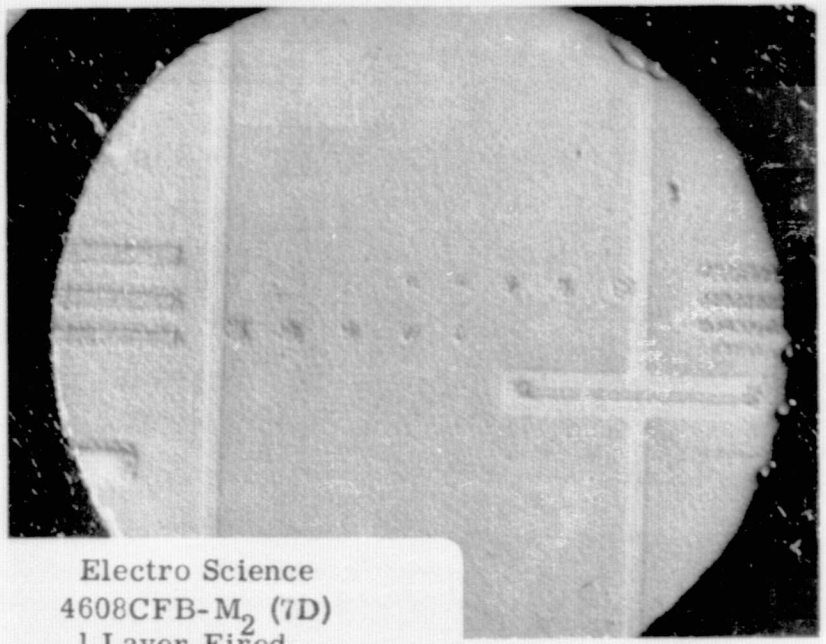
Electro Science
4608C (6D)
2 Layers Unfired
FIGURE 2.12-23



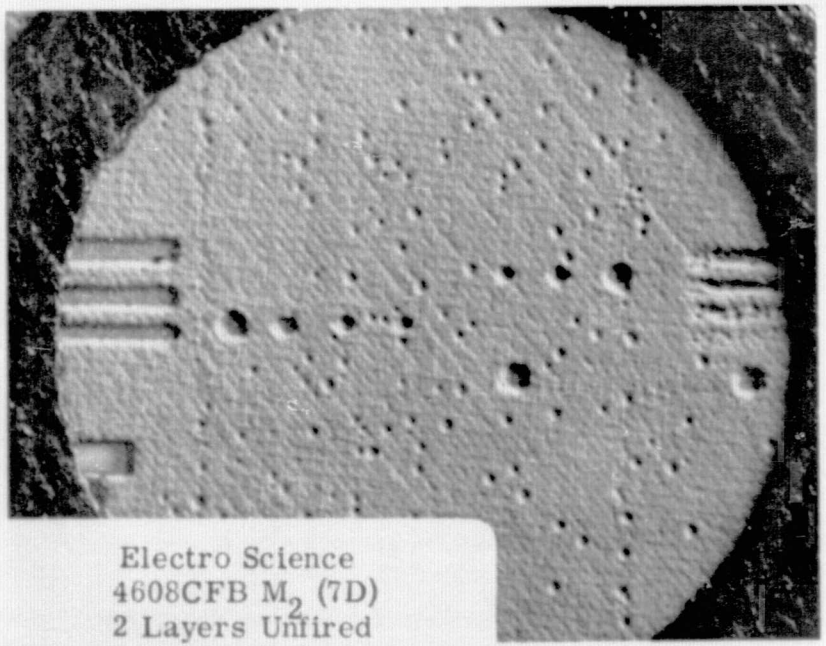
Electro Science
4608C (6D)
2 Layers Fired
FIGURE 2.12-24



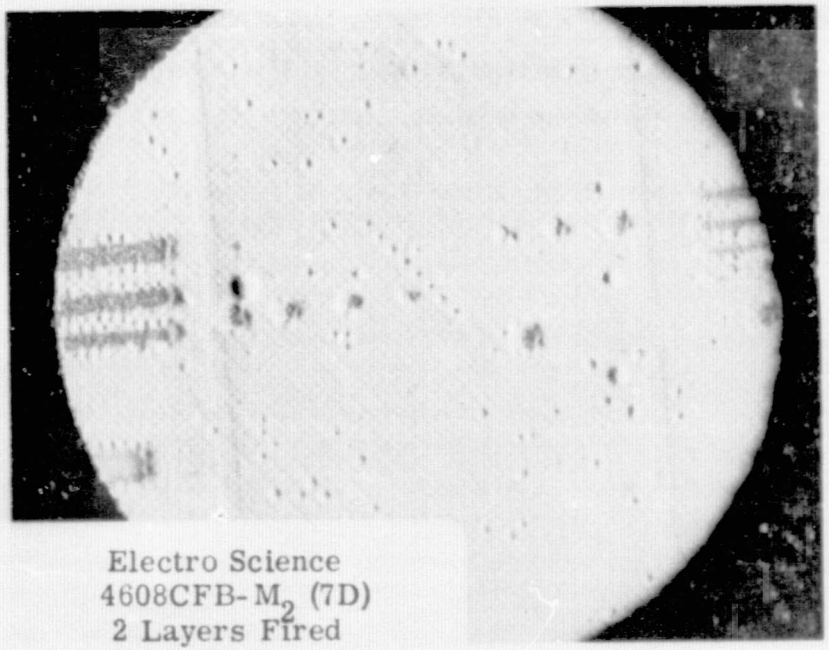
Electro Science
4608CFB-M_2 (7D)
1 Layer Unfired
FIGURE 2.12-25



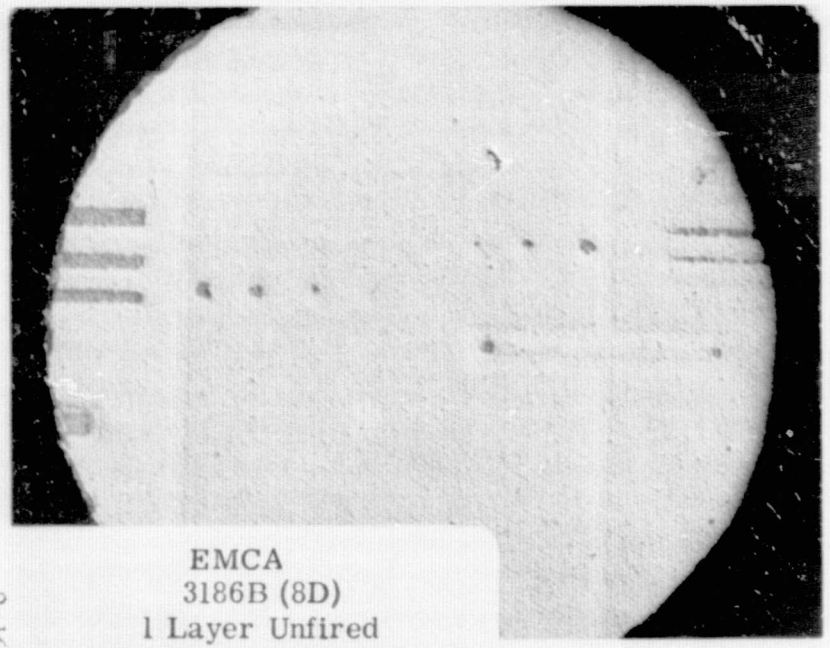
Electro Science
4608CFB-M_2 (7D)
1 Layer Fired
FIGURE 2.12-26



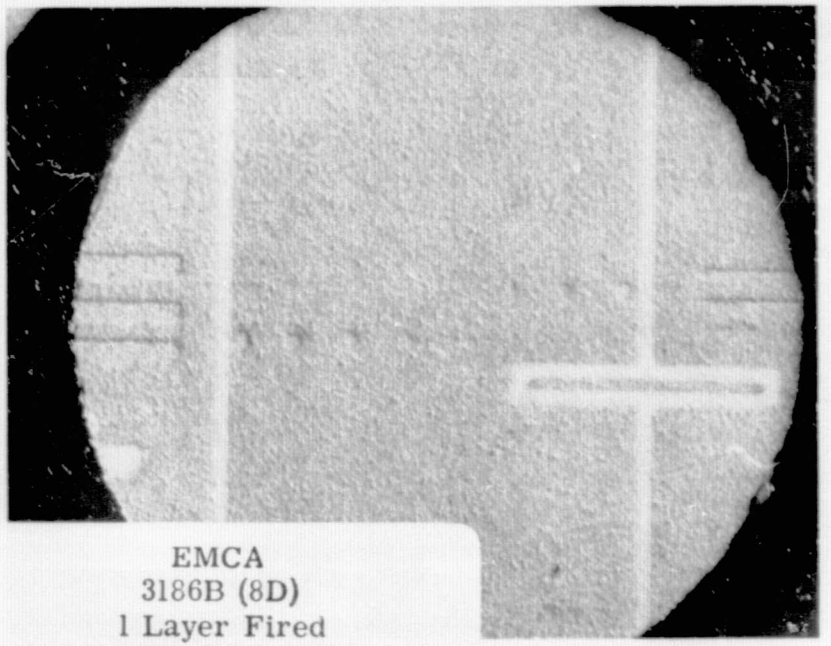
Electro Science
4608CFB M_2 (7D)
2 Layers Unfired
FIGURE 2.12-27



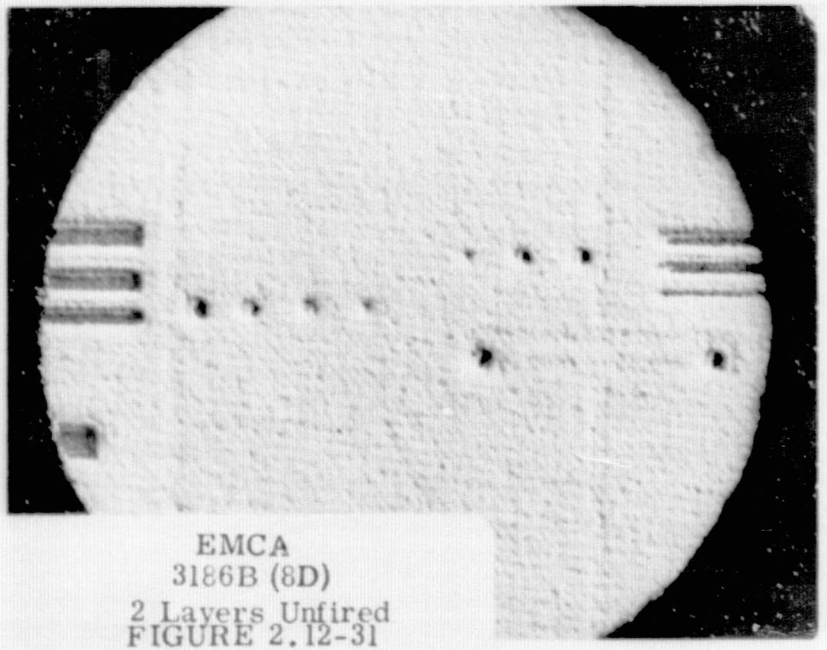
Electro Science
4608CFB-M_2 (7D)
2 Layers Fired
FIGURE 2.12-28



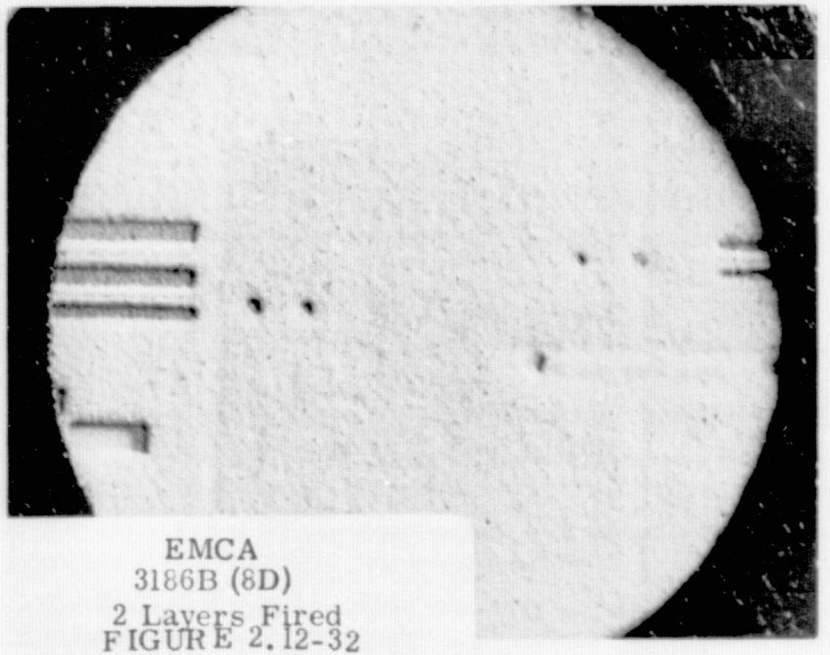
EMCA
3186B (8D)
1 Layer Unfired
FIGURE 2.12-29



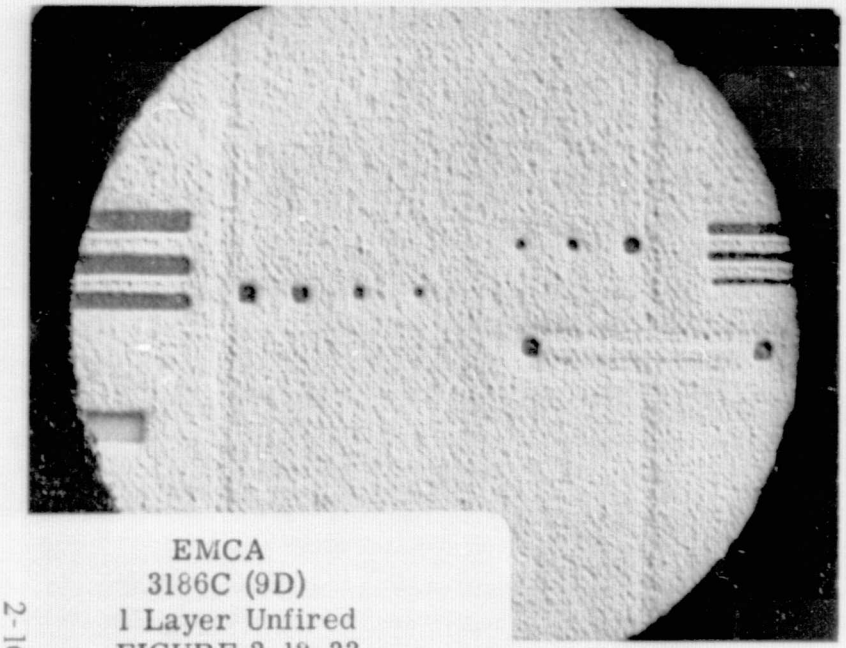
EMCA
3186B (8D)
1 Layer Fired
FIGURE 2.12-30



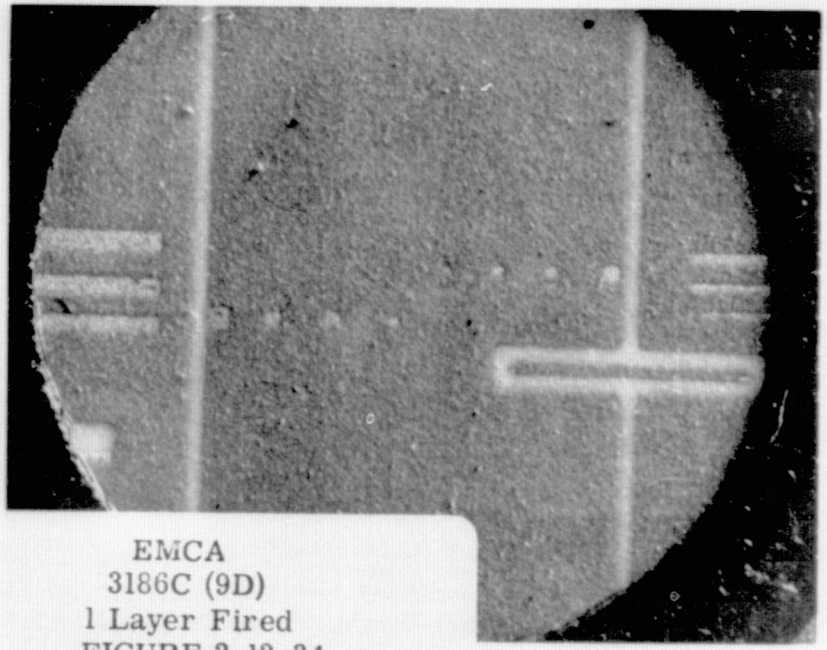
EMCA
3186B (8D)
2 Layers Unfired
FIGURE 2.12-31



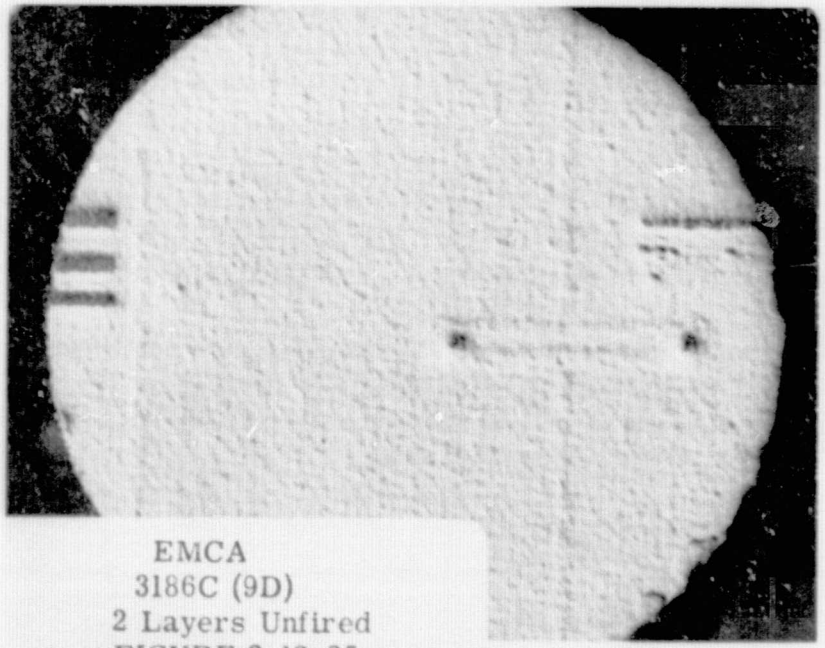
EMCA
3186B (8D)
2 Layers Fired
FIGURE 2.12-32



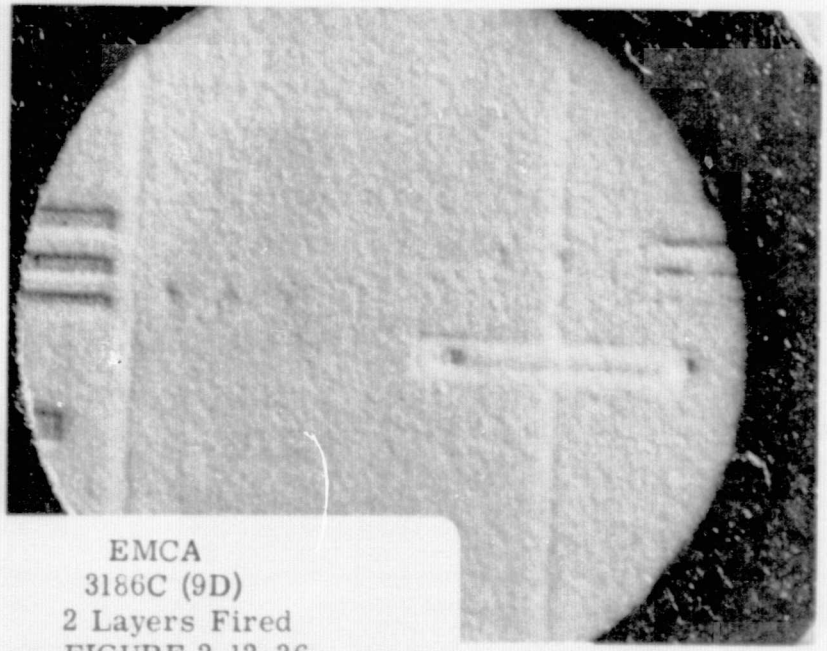
EMCA
3186C (9D)
1 Layer Unfired
FIGURE 2.12-33



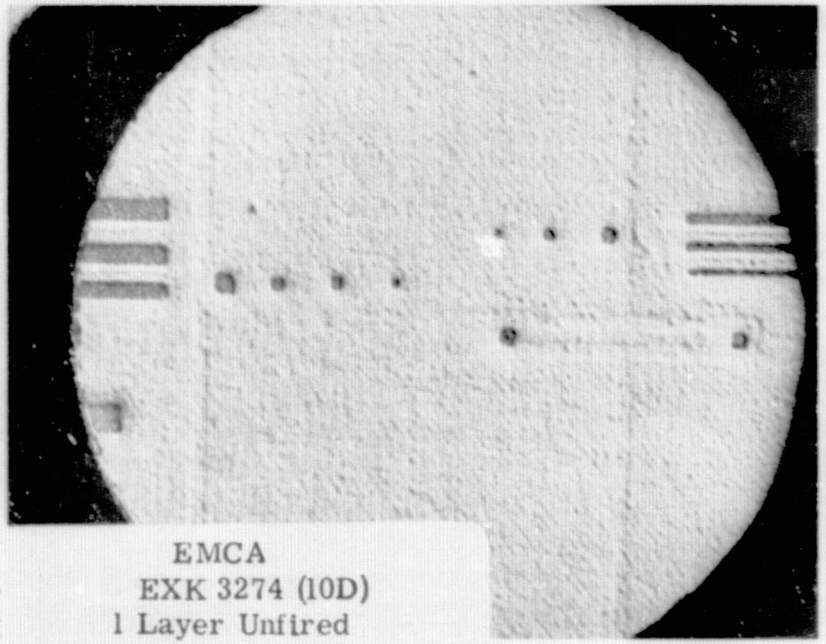
EMCA
3186C (9D)
1 Layer Fired
FIGURE 2.12-34



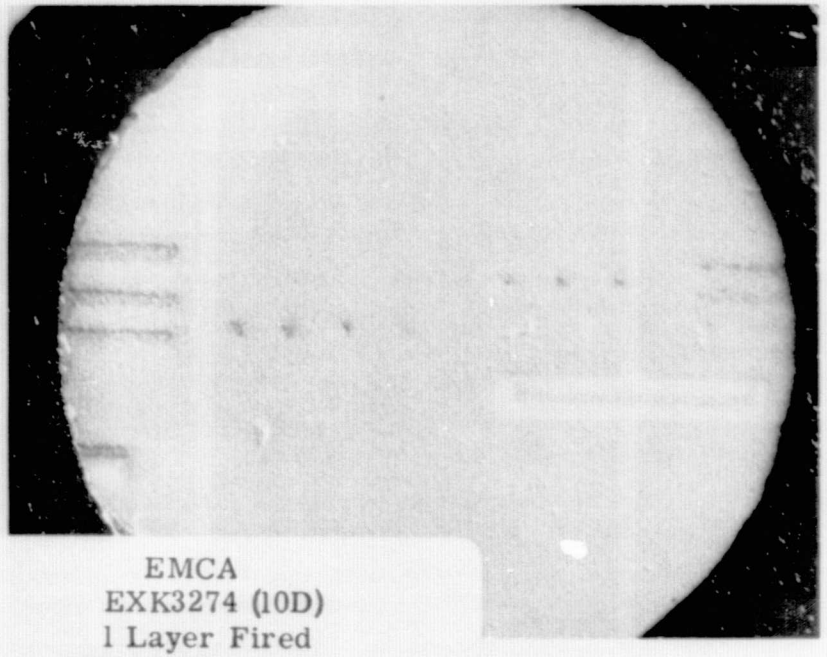
EMCA
3186C (9D)
2 Layers Unfired
FIGURE 2.12-35



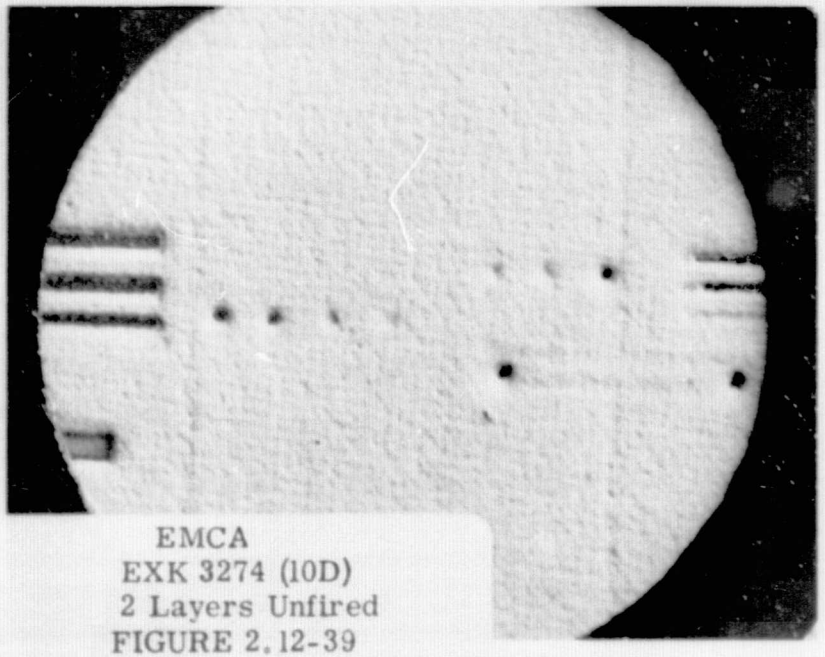
EMCA
3186C (9D)
2 Layers Fired
FIGURE 2.12-36



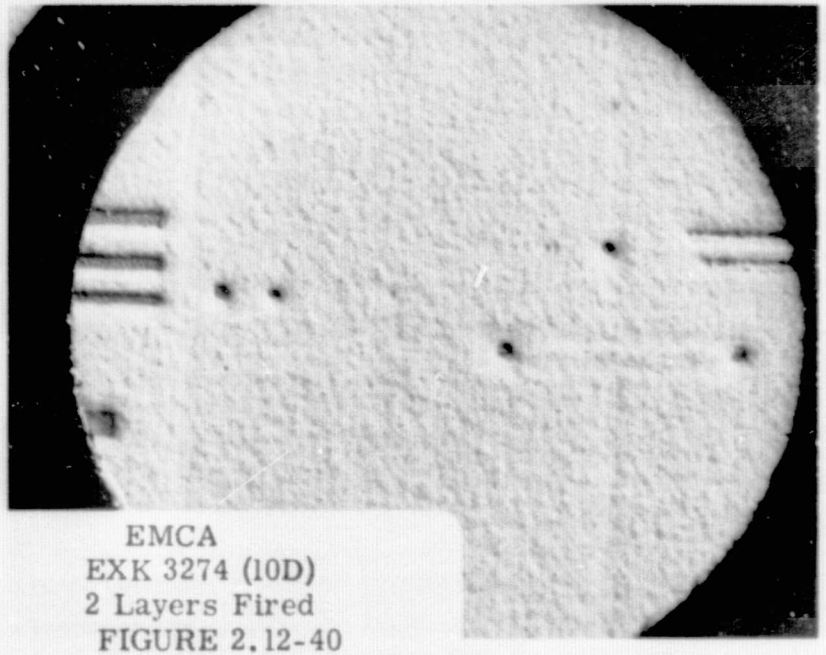
EMCA
EXK 3274 (10D)
1 Layer Unfired
FIGURE 2.12-37



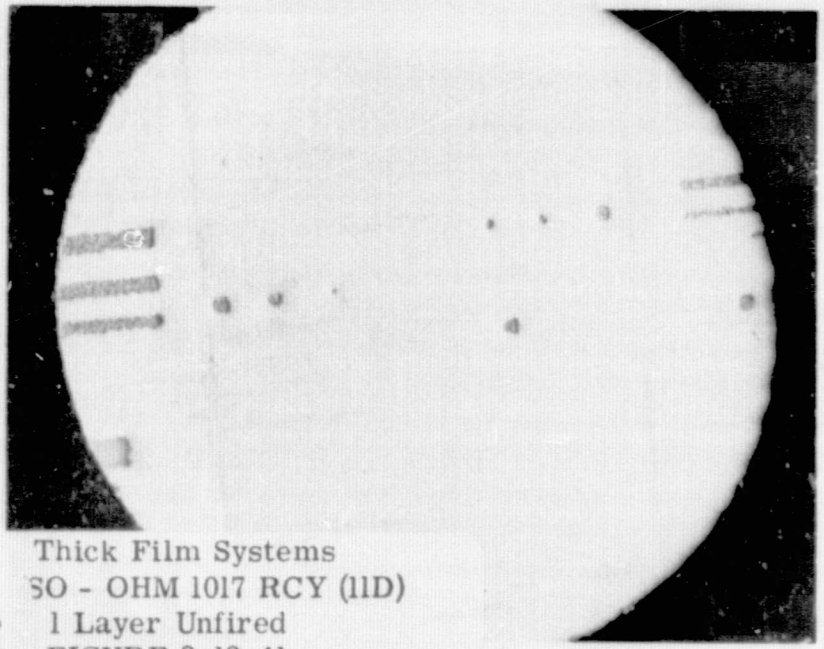
EMCA
EXK3274 (10D)
1 Layer Fired
FIGURE 2.12-38



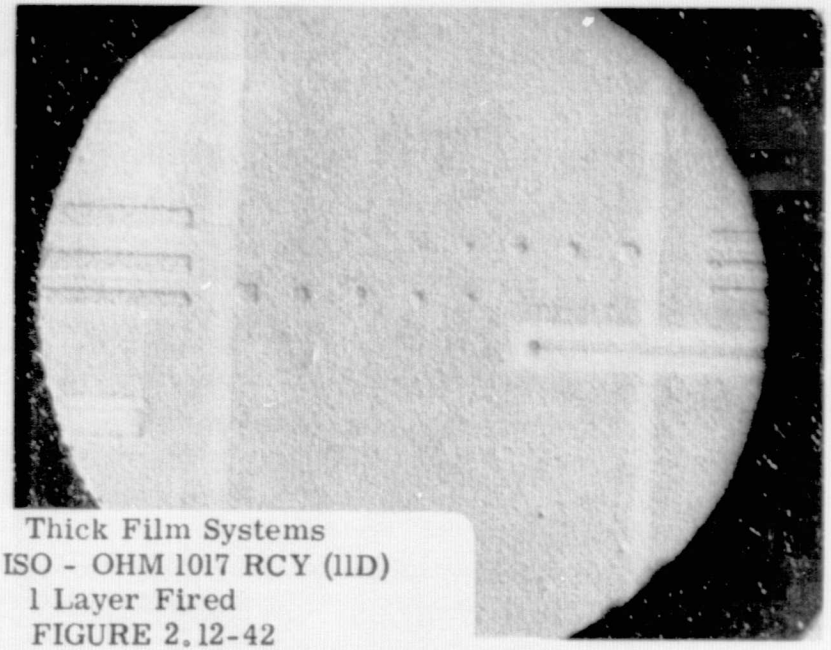
EMCA
EXK 3274 (10D)
2 Layers Unfired
FIGURE 2.12-39



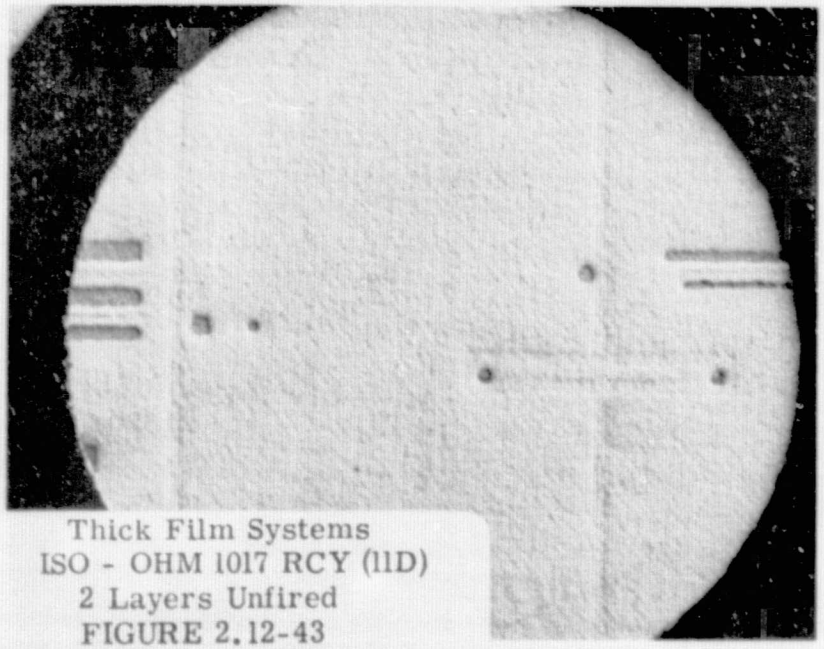
EMCA
EXK 3274 (10D)
2 Layers Fired
FIGURE 2.12-40



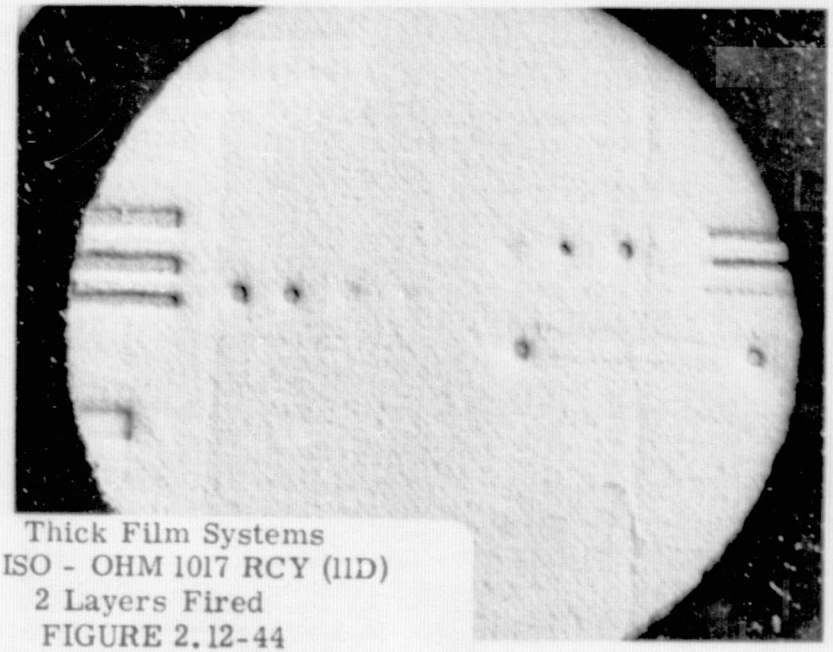
Thick Film Systems
ISO - OHM 1017 RCY (11D)
1 Layer Unfired
FIGURE 2.12-41



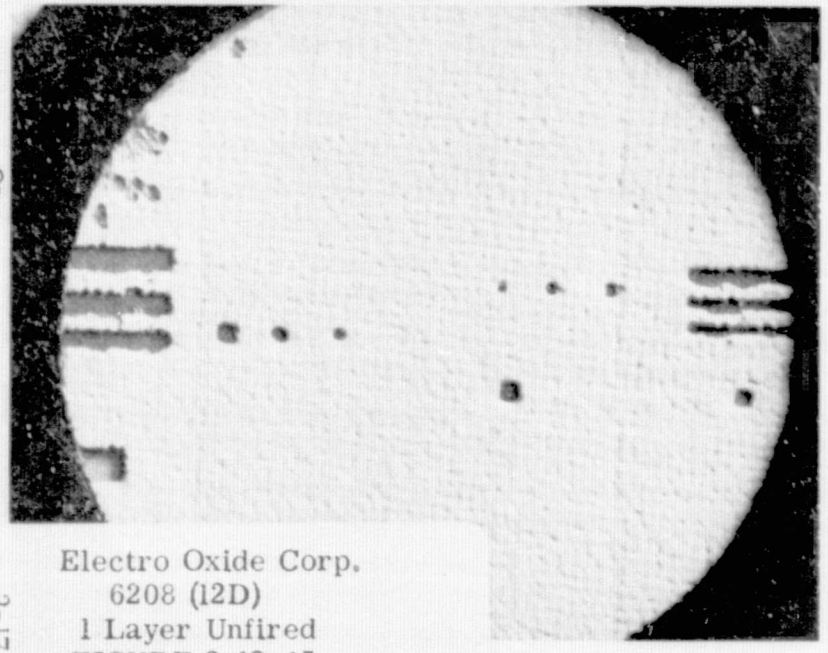
Thick Film Systems
ISO - OHM 1017 RCY (11D)
1 Layer Fired
FIGURE 2.12-42



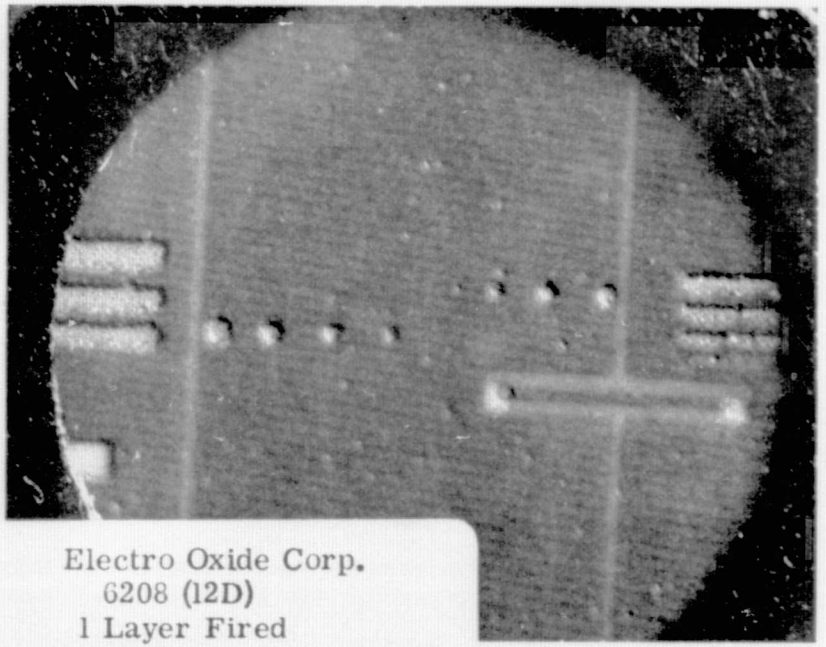
Thick Film Systems
ISO - OHM 1017 RCY (11D)
2 Layers Unfired
FIGURE 2.12-43



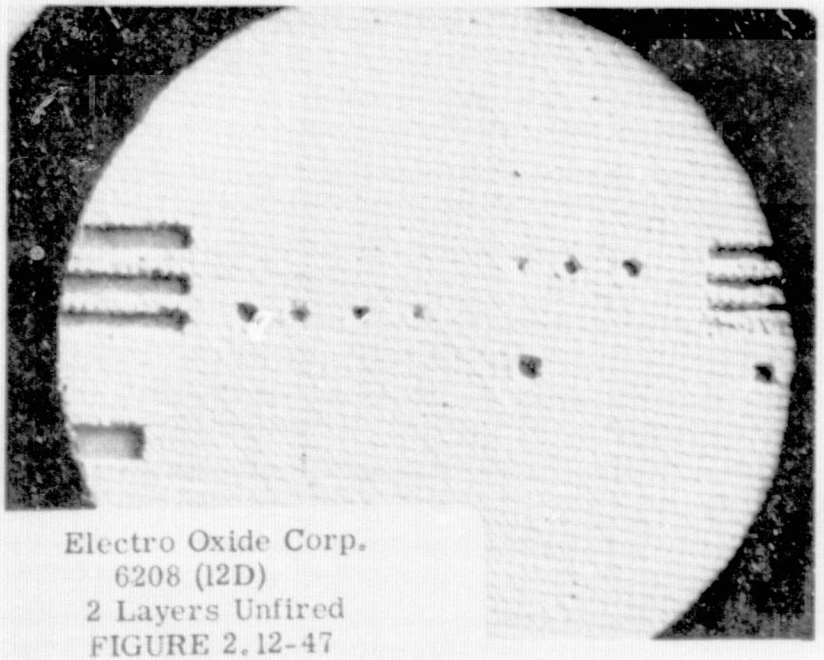
Thick Film Systems
ISO - OHM 1017 RCY (11D)
2 Layers Fired
FIGURE 2.12-44



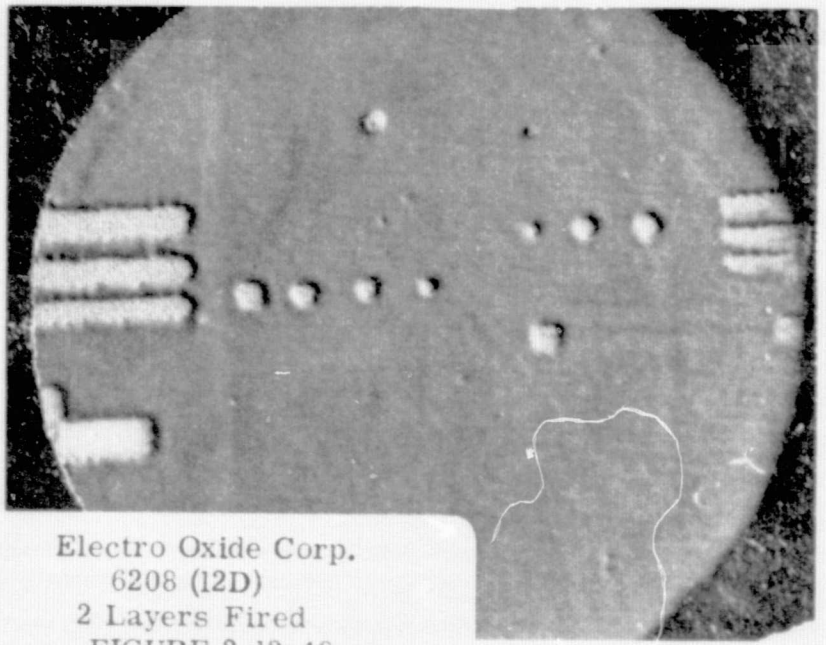
Electro Oxide Corp.
6208 (12D)
1 Layer Unfired
FIGURE 2.12-45



Electro Oxide Corp.
6208 (12D)
1 Layer Fired
FIGURE 2.12-46



Electro Oxide Corp.
6208 (12D)
2 Layers Unfired
FIGURE 2.12-47



Electro Oxide Corp.
6208 (12D)
2 Layers Fired
FIGURE 2.12-48

2.12.2 Conductor Compositions

The conductor compositions received were evaluated after being screened and fired, both on bare substrate and over the various dielectric compositions included in the program. The manufacturers recommended procedures for processing were followed to assure compliance with the optimum conditions.

The fine line conductor pattern described in the Test Pattern Utilization section (2.8) was used with a stainless steel screen of 325 mesh. Measurements taken included line definition and resistivity of fired conductor patterns.

2.12.2.1 Conductors Printed and Fired on Bare Substrate

2.12.2.1.1 Thick Film Systems Gold 401.7 (1C)

Figure 2.12.49

This conductor system was of the so-called "fritless" material family. The fired conductor had a bright gold, metallic luster, characteristic of these materials. The fired conductor material had a line resolution of .008 inch width and spacing with .006 inch capability with extreme care. The average line resistivity based on .008 inch wide lines was .0038 Ω □ .

2.12.2.1.2 Thick Film Systems Gold 3009 (2C)

Figure 2.12-50

This conductor material produced a dense continuous line with a definition capability of .004 inch lines with .002 inch wide lines possible in the major portion of screenings. The average line resistivity measured was .0071 Ω/□ for .008 inch wide lines.

2.12.2.1.3 Engelhard Gold 2894 (3C)

Figure 2.12-51

Some difficulty was encountered in processing this conductor as it had a tendency to stick to the screen and pull off of the substrate. The line resolution observed was .008 inch wide with an average of .0043 Ω/□ resistivity for this width.

2.12.2.1.4 Engelhard Gold 2789 (4C)

Figure 2.12-52

This conductor system was of the fritless type and listed as a molecular bonding conductor system. The conductor system produced by screen and fire techniques was of a very dense, highly lustrous character. The line resolution was .004 inches wide and the average line resistivity was .009 Ω/□ for .008 inch wide lines.

2.12.2.1.5 Engelhard Gold 1560 (5C)

Figure 2.12-53

The conductor system produced with this paste was very bright and dense with a pure gold appearance. The line resolution observed was .004 inches wide with an average line resistivity of .005 Ω/□ for .008 inch wide lines.

2.12.2.1.6 DuPont Gold 9260 (6C)

Figure 2.12-54

The conductor patterns produced with this material were very smooth and consistent. The line resolution observed was .004 inches with an average line resistivity of .0051 Ω/□ for .008 inch wide lines.

2.12.2.1.7 DuPont Gold 8237 (7C)

Figure 2.12-55

This conductor system produced smooth even lines but had a tendency to reduce line spacing due to its wetting characteristics. The line resolution

observed was .004 inch wide lines but minimum spacing should be kept to .006 inches. Average line resistivity for .008 inch lines was .0084 Ω/□ .

2.12.2.1.8 Electro Science Gold 8835-1B (8C)

Figure 2.12-56

The conductors produced with this material exhibited screen impressions which prevented achieving smooth continuous lines in smaller line widths. The average line resolution observed was .006 inches wide for long runs. The average line resistivity for .008 inch wide lines was .0064Ω/□ .

2.12.2.1.9 Electro Science Gold 8835 (9C)

Figure 2.12-57

This conductor system was very similar to the 8835-1B system with the exception that it had a greater tendency to "heal" screen impressions. The resultant fired conductors were smooth and continuous with a line resolution of .004 inch width and with an average line resistivity of .0095Ω/□ for .008 inch wide lines.

2.12.2.1.10 EMCA Gold EXK3264 (10C)

Figure 2.12-58

The conductor lines produced with this material retained the screen impressions resulting in a somewhat coarse line definition. The smaller lines had continuity but exhibited somewhat inconsistent line thickness. The line resolution observed was .004 inches wide with .006 considered a more consistent line width. The average line resistivity for .008 inch wide lines was .0071 Ω/□ .

2.12.2.1.11 DuPont Platinum Gold 8653 (11C)

Figure 2.12-59

This conductor system produced excellent lines at .004 inches but spacing was a problem due to closing in by the material. A line spacing of .006 inches is recommended. The average line resistivity observed was .1651Ω/□ for .008 inch wide lines.

2.12.2.1.12 EMCA Platinum Gold EXK3283 (12C)

Figure 2.12-60

This material had a very high viscosity which made screening difficult. Extended periods of settling did not result in screen impression healing. The fired conductors were very thin and open areas in all lines prevented resistivity measurements.

2.12.2.1.13 Sel-Rex Company Gold DX 799 (13C)

Figure 2.12-61

Definition for lines of .006 inches and above was excellent with this material with .004 inches wide being inconsistent in texture. The average line resistivity observed with this material for .008 inch wide lines was .0049 Ω/□ .

2.12.2.1.14 Electro Oxide Corporation Gold 6990 (14C)

Figure 2.12-62

This material was quite high in viscosity resulting in some difficulty in screening. The fired film had areas of thin metallization resulting from the inability to heal screen impressions. All .006 inch wide lines had continuity but the thin sections made line widths below .008 inch suspect as to integrity. The average line resistivity for .008 inch wide lines was .008 Ω/□ .

2.12.2.1.15 Thick Film Systems Copper EX513 (15C)

Figure 2.12-63

Results are confidential.

2.12.2.1.16 Engelhard Nickel 2884 (25C)

Figure 2.12-64

This material was of the non-noble fritless conductor system. The fired conductor pattern appeared to be somewhat expanded in comparison with

the dried unfired conductor. Line definition can be printed to .004 inch wide but spacing should not be less than .008 due to intrusion of conductor material during drying and firing. The average line resistivity observed was .165Ω/□ for .008 inch wide lines.

2.12.2.1.17 Engelhard Aluminum 2746 (3SC)

Figure 2.12-65

The fired conductors of this material appeared quite similar to that of the 2884 nickel. Difficulty in screening was encountered due to viscosity of paste and the tendency of the material to wet the substrate. Line definition of .006 inches wide was possible but line spacing should be maintained at a minimum of .010 inches. The average line resistivity cannot be calculated due to inconsistency of samples resulting from line shorts.

2.12.2.1.18 Electro Science Nickel 2502 (4SC)

Figure 2.12-66

This conductor system required a hydrogen atmosphere during firing. The results are not published here as it is not considered a normally processed material.

2.12.2.1.19 Cermalloy Copper 7029 (5SC)

Figure 2.12-67

This material required special processing procedures and results are not published in this report.

2.12.2.1.20 Cermalloy Nickel 7028 (6SC)

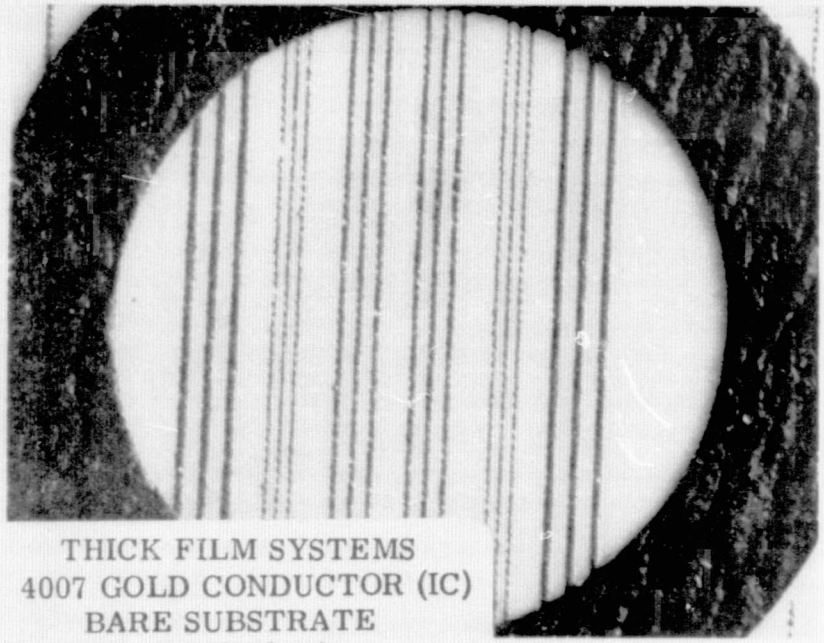
Figure 2.12-68

This material required special processing procedures. Therefore, the results will not be published in this report.

2.12.2.1.21 EMCA Nickel 6500 (7SC)

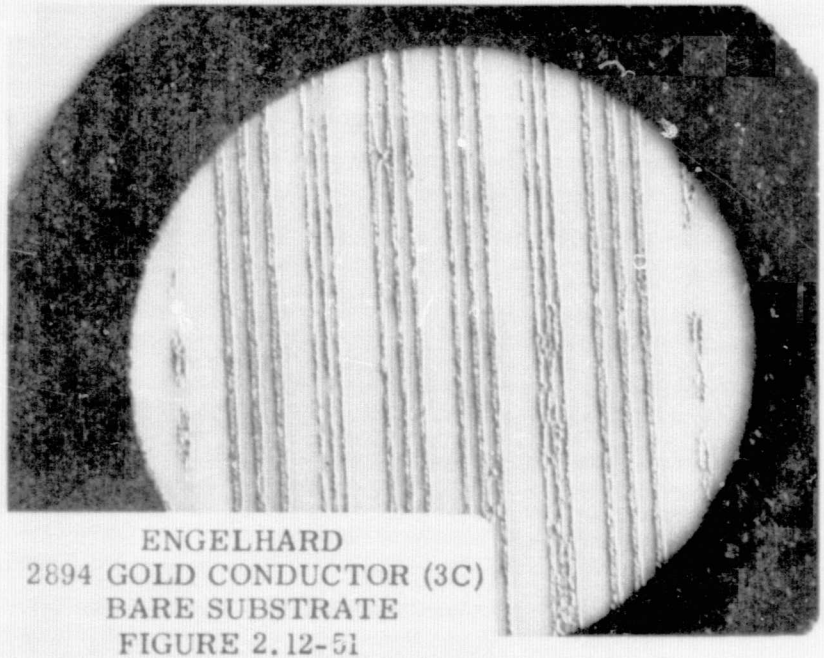
Figure 2.12-69

This material required special processing procedures and results will not be published in this report.

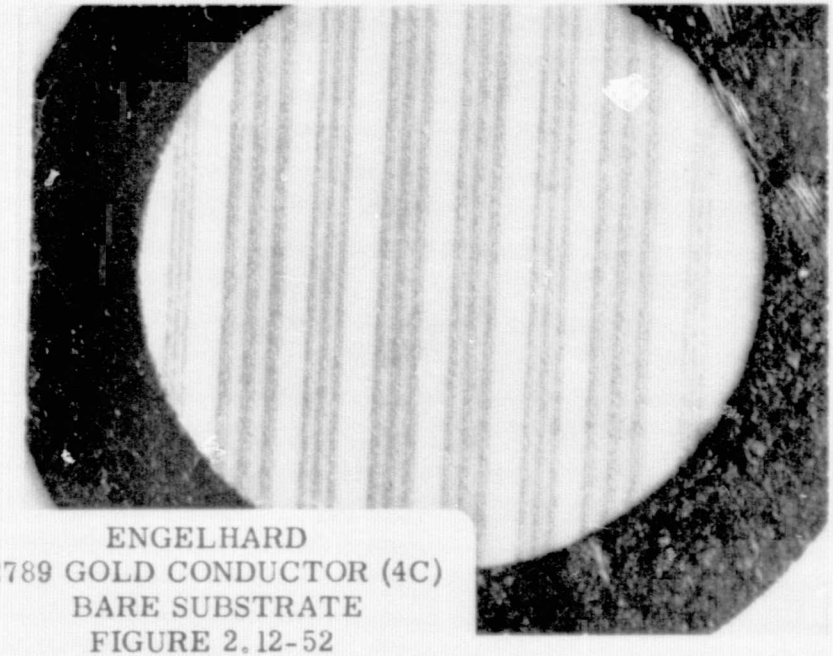


THICK FILM SYSTEMS
4007 GOLD CONDUCTOR (IC)
BARE SUBSTRATE
FIGURE 2.12-49

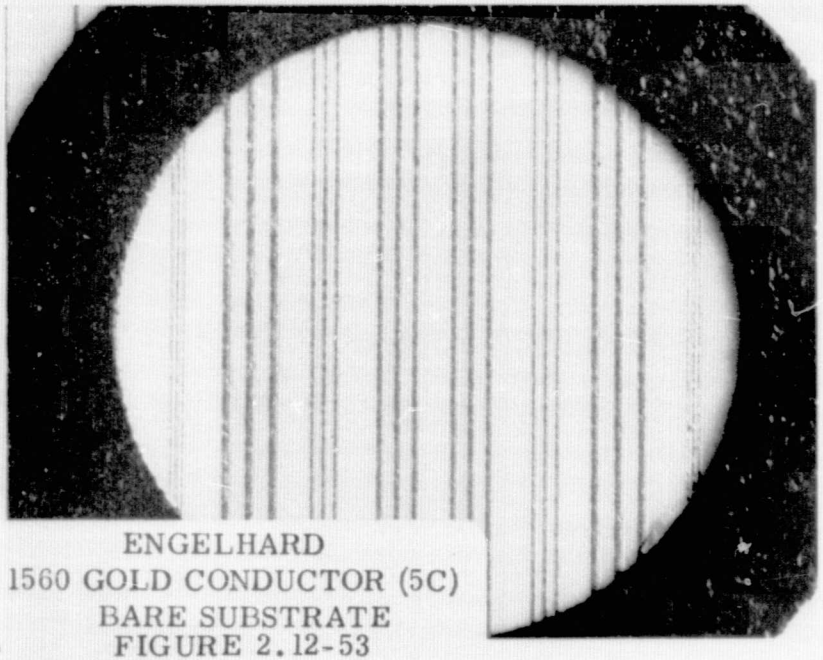
THICK FILM SYSTEMS
3009 GOLD CONDUCTOR (2C)
BARE SUBSTRATE
FIGURE 2.12-50



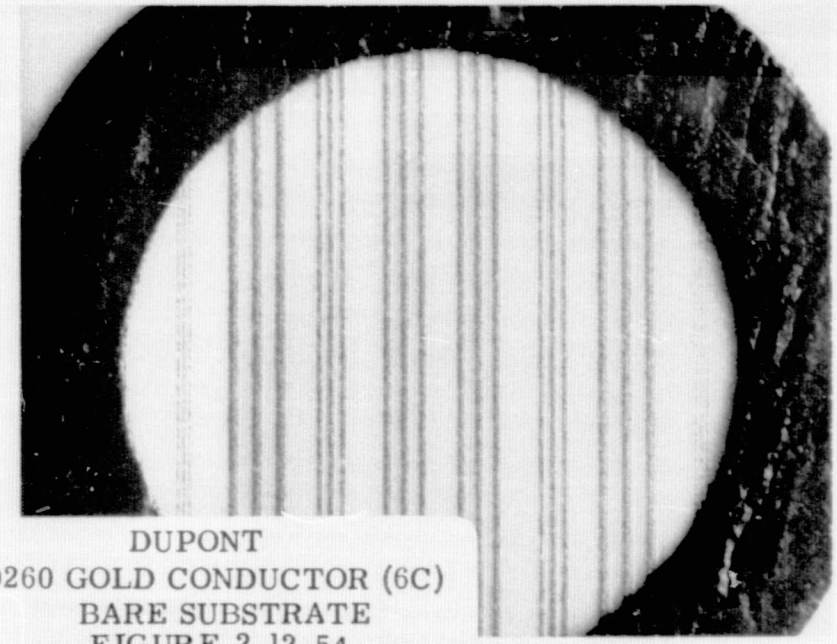
ENGELHARD
2894 GOLD CONDUCTOR (3C)
BARE SUBSTRATE
FIGURE 2.12-51



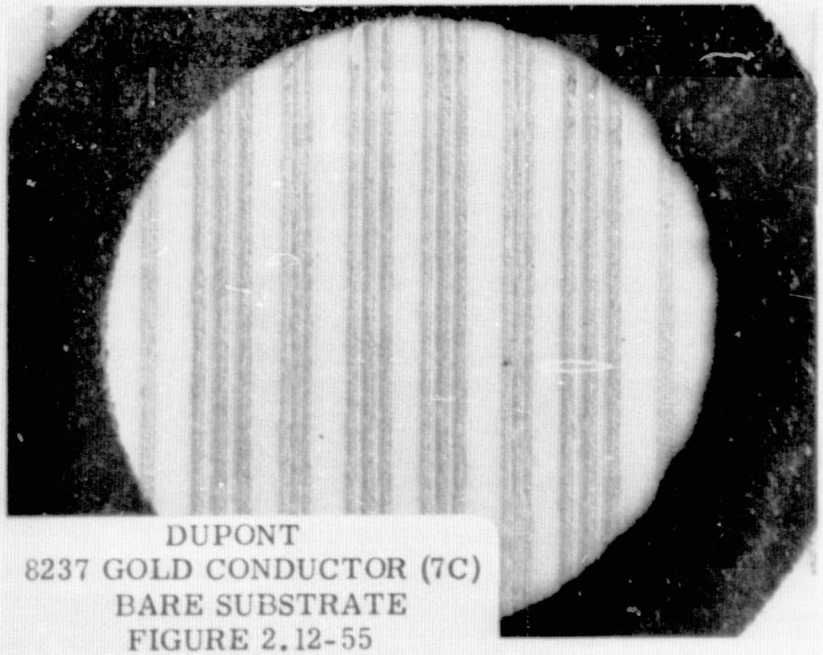
ENGELHARD
2789 GOLD CONDUCTOR (4C)
BARE SUBSTRATE
FIGURE 2.12-52



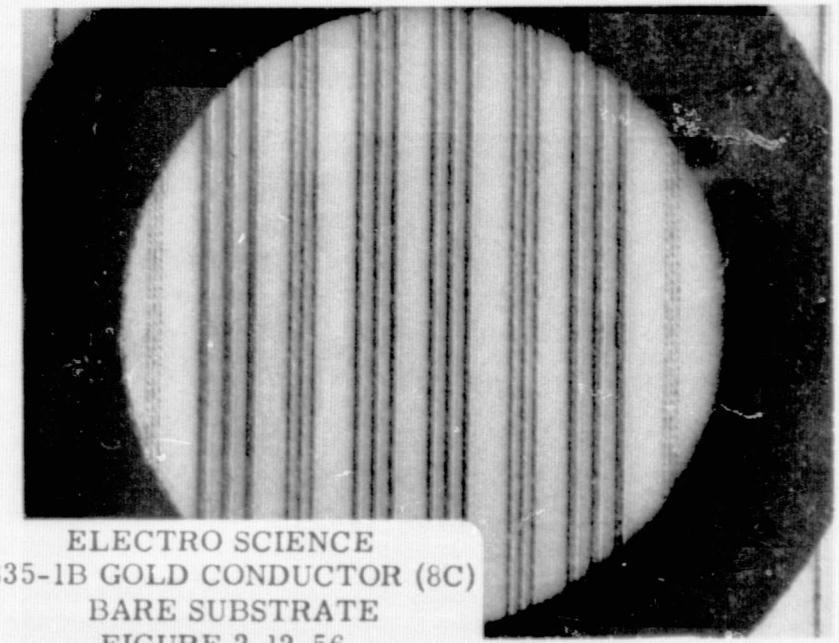
ENGELHARD
1560 GOLD CONDUCTOR (5C)
BARE SUBSTRATE
FIGURE 2.12-53



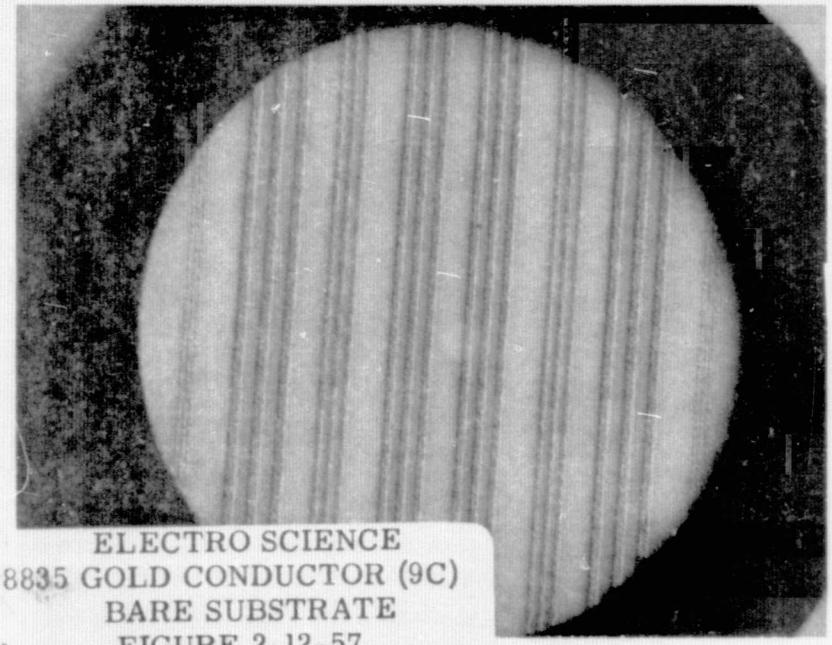
DUPONT
9260 GOLD CONDUCTOR (6C)
BARE SUBSTRATE
FIGURE 2.12-54



DUPONT
8237 GOLD CONDUCTOR (7C)
BARE SUBSTRATE
FIGURE 2.12-55



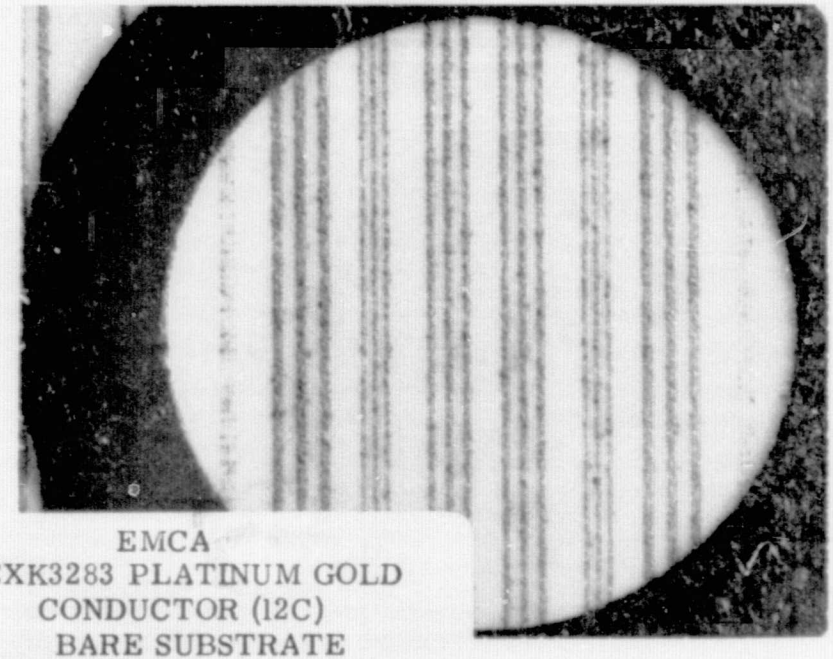
ELECTRO SCIENCE
8835-1B GOLD CONDUCTOR (8C)
BARE SUBSTRATE
FIGURE 2.12-56



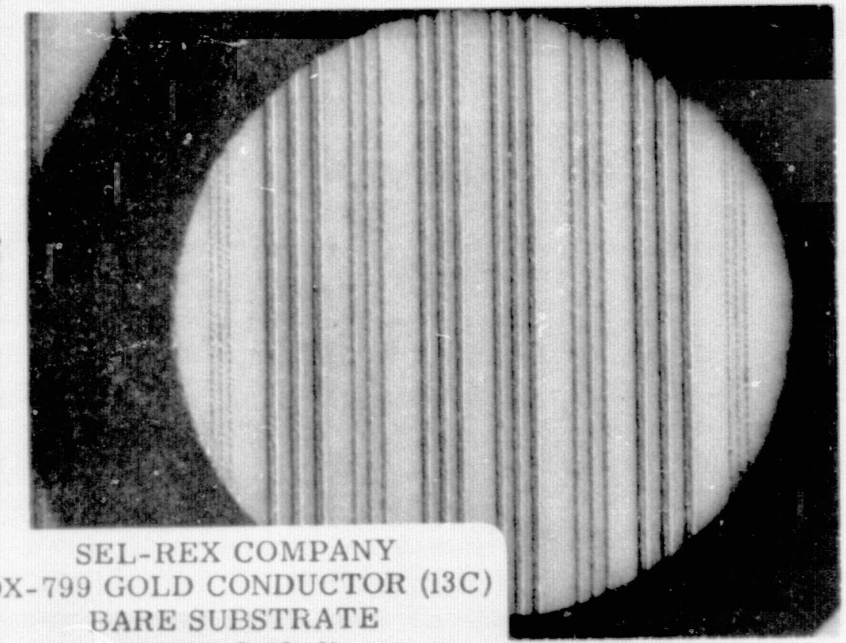
ELECTRO SCIENCE
8835 GOLD CONDUCTOR (9C)
BARE SUBSTRATE
FIGURE 2.12-57

EMCA
EXK3264 GOLD CONDUCTOR (10C)
BARE SUBSTRATE
FIGURE 2.12-58

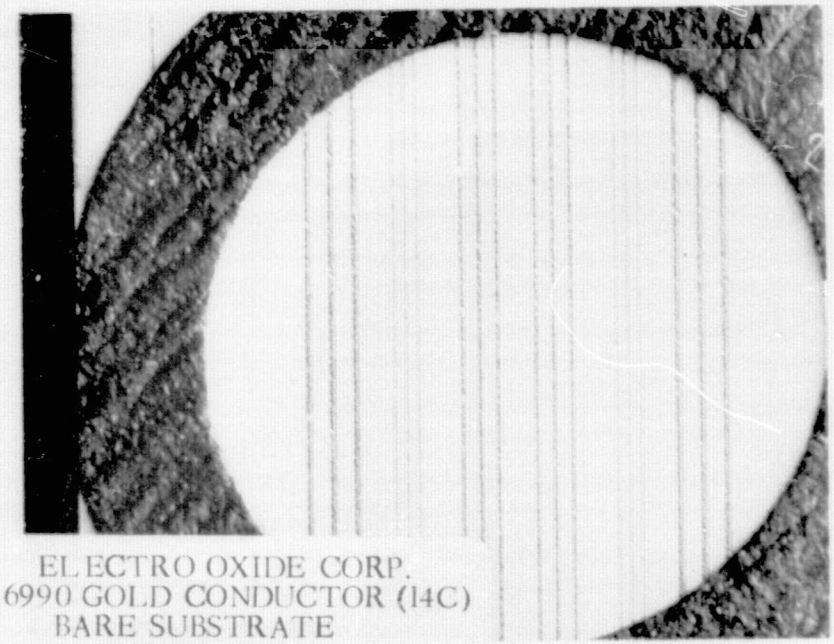
DUPONT
8653 PLATINUM GOLD
CONDUCTOR (11C)
BARE SUBSTRATE
FIGURE 2.12-59



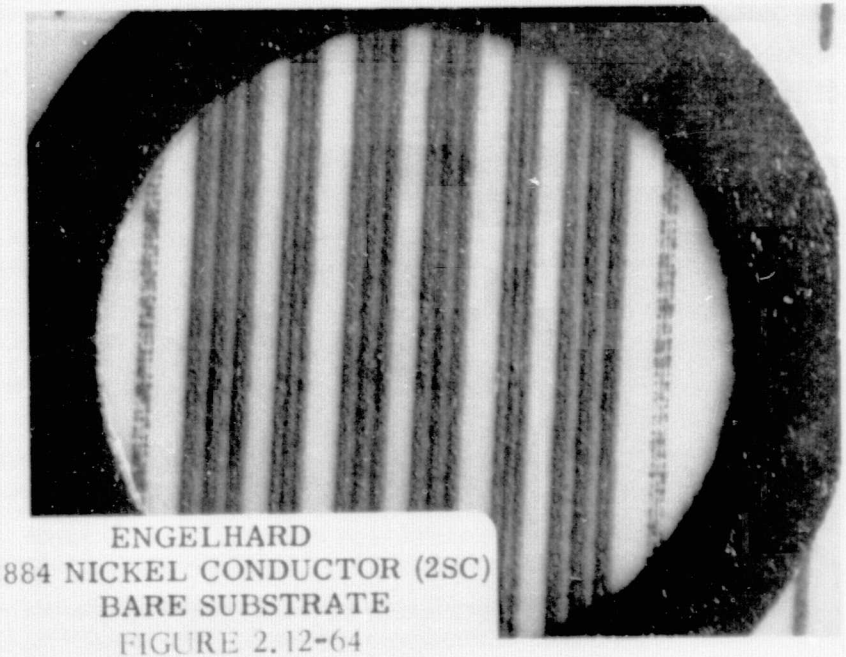
EMCA
EXK3283 PLATINUM GOLD
CONDUCTOR (12C)
BARE SUBSTRATE
FIGURE 2.12-60



SEL-REX COMPANY
DX-799 GOLD CONDUCTOR (13C)
BARE SUBSTRATE
FIGURE 2.12-61

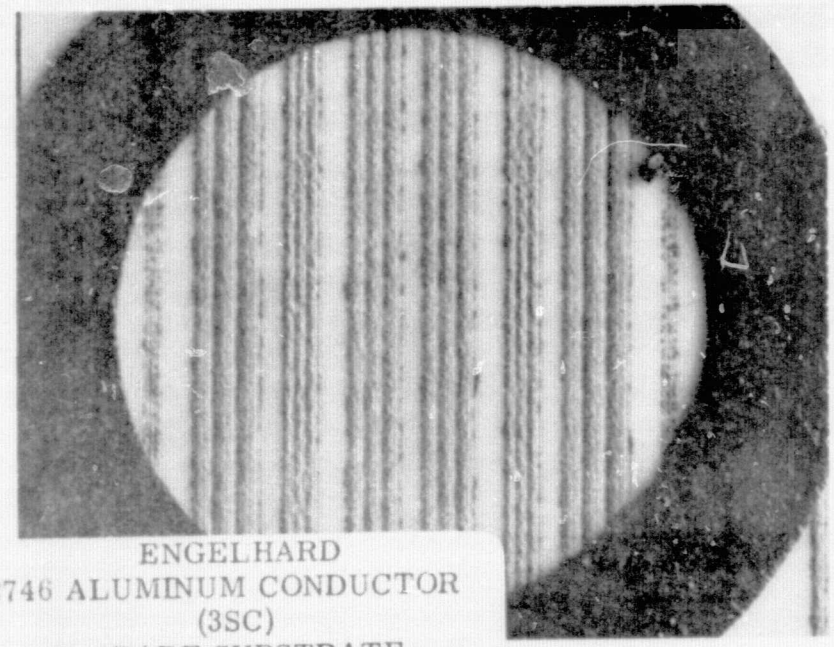


ELECTRO OXIDE CORP.
6990 GOLD CONDUCTOR (14C)
BARE SUBSTRATE
FIGURE 2.12-62

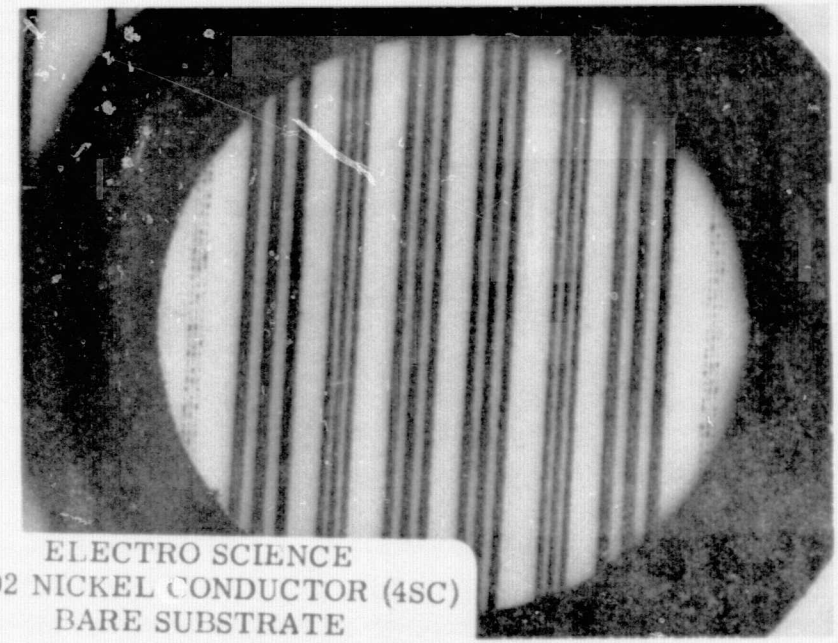


ENGELHARD
2884 NICKEL CONDUCTOR (2SC)
BARE SUBSTRATE
FIGURE 2.12-64

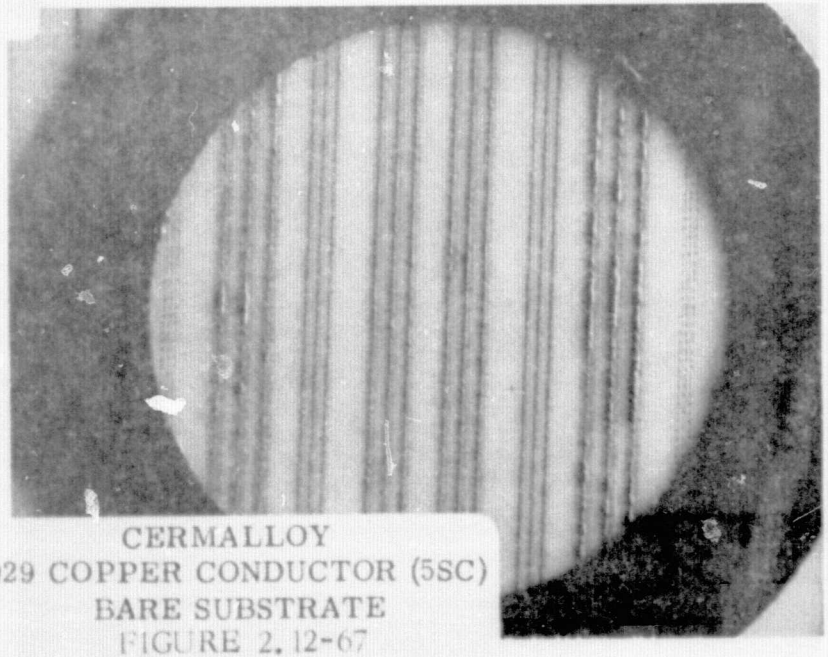
THICK FILM SYSTEMS
EX513 COPPER CONDUCTOR
(1SC)
BARE SUBSTRATE
FIGURE 2.12-63



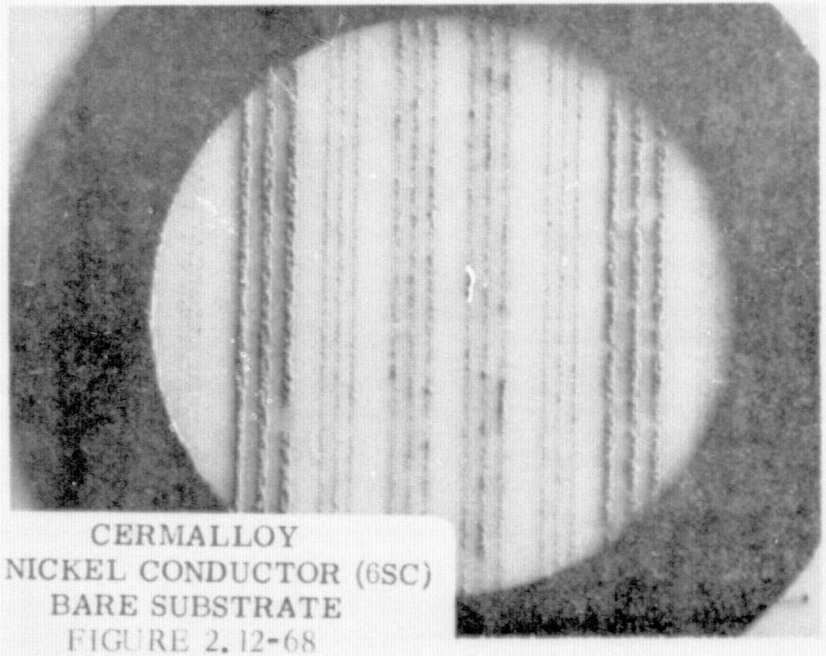
ENGELHARD
2746 ALUMINUM CONDUCTOR
(3SC)
BARE SUBSTRATE
FIGURE 2.12-65



ELECTRO SCIENCE
2502 NICKEL CONDUCTOR (4SC)
BARE SUBSTRATE
FIGURE 2.12-66



CERMALLOY
7029 COPPER CONDUCTOR (5SC)
BARE SUBSTRATE
FIGURE 2.12-67



CERMALLOY
7028 NICKEL CONDUCTOR (6SC)
BARE SUBSTRATE
FIGURE 2.12-68

EMCA
6500 NICKEL CONDUCTOR (7SC)
BARE SUBSTRATE
FIGURE 2.12-69

2.12.2.2 Conductors Fired Over Dielectric

The quantity of samples developed for the combinations study prohibits a detailed analysis of all of the results at this writing. The following illustrations are presented for comparison.

2.12.2.2 1 Thick Film Systems Gold 4007 (1C) fired over Thick Film Systems dielectric 1017 RCA (1D). Figure 2.12-70.

2.12.2.2.2 Thick Film Systems Gold 4007 (1C) fired over Thick Film Systems dielectric 1005 TCG (2D). Figure 2.12-71.

2.12.2.2.3 Thick Film Systems Gold 4007 (1C) fired over Engelhard dielectric A-2835 (3D) Figure 2.12-72.

2.12.2.2.4 Thick Film Systems Gold 4007 (1C) fired over DuPont dielectric 8299 (4D). Figure 2.12-73.

2.12.2.2.5 Thick Film Systems Gold 4007 (1C) fired over DuPont 9429 dielectric (5D) Figure 2.12-74.

2.12.2.2.6 Thick Film Systems Gold 4007 (1C) fired over Electro Science Corporation dielectric 4608C (6D) Figure 2.12-75.

2.2.2.2.7 Thick Film Systems Gold 4007 (1C) fired over Electro Science Corporation dielectric 4608 CFB-M2 (7D) Figure 2.12-76.

2.12.2.2.8 Thick Film Systems Gold 4007 (1C) fired over EMCA dielectric 8186B (8D) Figure 2.12-77.

2.12.2.2.9 Thick Film Systems Gold 4007 (1C) fired over EMCA dielectric 3186C (9D). Figure 2.12-78.

2.12.2.2.10 Thick Film Systems Gold 4007 (1C) fired over EMCA dielectric EXK3274 (10D). Figure 2.12-79.

2.12.2.2.11 Thick Film Systems Gold 4007 (1C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-80.

2.12.2.2.12 Thick Film Systems Gold 4007 (1C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-81.

2.12.2.2.13 Thick Film Systems Gold 3009 (2C) fired over Thick Film Systems dielectric 1017 RCA, (1D), Figure 2.12-82.

2.12.2.2.14 Thick Film Systems Gold 3009 (2C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-83.

2.12.2.2.15 Thick Film Systems Gold 3009 (2C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-84.

2.12.2.2.16 Thick Film Systems Gold 3009 (2C) fired over DuPont dielectric 8299 (4D), Figure 2.12-85.

2.12.2.2.17 Thick Film Systems Gold 3009 (2C) fired over DuPont dielectric 9429 (5D), Figure 2.12-86.

2.12.2.2.18 Thick Film Systems Gold 3009 (2C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-87.

2.12.2.2.19 Thick Film Systems Gold 3009 (2C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-88.

2.12.2.2.20 Thick Film Systems Gold 3009 (2C) fired over EMCA dielectric 3186B (8D), Figure 2.12-89.

2.12.2.2.21 Thick Film Systems Gold 3009 (2C) fired over EMCA dielectric 3186C, (9D), Figure 2.12-90.

2.12.2.2.22 Thick Film Systems Gold 3009 (2C) fired over EMCA dielectric EXK3274 (10D) Figure 2.12-91.

2.12.2.2.23 Thick Film Systems Gold 3009 (2C) fired over Thick Film Systems dielectric 1017 RCY (11D). Figure 2.12-92.

2.12.2.2.24 Thick Film Systems Gold 3009 (2C) fired over Electro Oxide Corporation 6208 (12D). Figure 2.12-93.

2.12.2.2.25 Engelhard Gold A2894 (3C) fired over Thick Film Systems dielectric 1017 RCA (1D). Figure 2.12-94.

2.12.2.2.26 Engelhard Gold A2894 (3C) fired over Thick Film Systems dielectric 1005 TCG (2D). Figure 2.12-95.

2.12.2.2.27 Engelhard Gold A2894 (3C) fired over Engelhard dielectric A-2835 (3D). Figure 2.12-96.

2.12.2.2.28 Engelhard Gold A2894 (3C) fired over DuPont dielectric 8299 (4D). Figure 2.12-97.

2.12.2.2.29 Engelhard Gold A2894 (3C) fired over DuPont dielectric 9429 (5D). Figure 2.12-98.

2.12.2.2.30 Engelhard Gold A2894 (3C) fired over Electro Science Corporation dielectric 6408C, (6D). Figure 2.12-99.

2.12.2.2.31 Engelhard Gold A2894 (3C) fired over Electro Science Corporation dielectric 6408 CFB-M2 (7D). Figure 2.12-100.

2.12.2.2.32 Engelhard Gold A2894 (3C) fired over EMCA dielectric 3186B (8D). Figure 2.12-101.

2.12.2.2.33 Engelhard Gold A2894 (3C) fired over EMCA dielectric 8186C (9D). Figure 2.12-102.

2.12.2.2.34 Engelhard Gold A2894 (3C) fired over EMCA dielectric EXK3274 (10D). Figure 2.12-103.

2 12.2.2.35 Engelhard Gold A2894 (3C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-104.

2.12.2.2.36 Engelhard Gold A2894 (3C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-105.

2.12.2.2.37 Engelhard Gold A-2789 (4C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-106.

2.12.2.2.38 Engelhard Gold A-2789 (4C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-107.

2.12.2.2.39 Engelhard Gold A-2789 (4C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-108.

2.12.2.2.40 Engelhard Gold A-2789 (4C) fired over DuPont dielectric 8299 (4D), Figure 2.12-109.

2.12.2.2.41 Engelhard Gold A-2789 (4C) fired over DuPont dielectric 9429 (5D), Figure 2.12-110.

2.12.2.2.42 Engelhard Gold A-2789 (4C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-111.

2.12.2.2.43 Engelhard Gold A-2789 (4C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-112.

2.12.2.2.44 Engelhard Gold A-2789 (4C) fired over EMCA dielectric 3186B (8D), Figure 2.12-113.

2.12.2.2.45 Engelhard Gold A-2789 (4C) fired over EMCA dielectric 3186C (9D), Figure 2.12-114.

2.12.2.2.46 Engelhard Gold A-2789 (4C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-115.

2.12.2.2.47 Engelhard Gold A-2789 (4C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-116.

2.12.2.2.48 Engelhard Gold A-2789 (4C) fired over Electro Oxide Corporation dielectric 6208 (12D) Figure 2.12-117.

2.12.2.2.49 Engelhard Gold A-1560 (5C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-118.

2.12.2.2.50 Engelhard Gold A-1560 (5C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-119.

2.12.2.2.51 Engelhard Gold A-1560 (5C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-120.

2.12.2.2.52 Engelhard Gold A-1560 (5C) fired over DuPont dielectric 8299 (4D), Figure 2.12-121.

2.12.2.2.53 Engelhard Gold A-1560 (5C) fired over DuPont dielectric 9429 (5D), Figure 2.12-122.

2.12.2.2.54 Engelhard Gold A-1560 (5C) fired over Electro Science Corporation dielectric 6408C (6D), Figure 2.12-123.

2.12.2.2.55 Engelhard Gold A-1560 (5C) fired over Electro Science Corporation dielectric 6408 CFB-M2 (7D), Figure 2.12-124.

2.12.2.2.56 Engelhard Gold A-1560 (5C) fired over EMCA dielectric 3186B (8D), Figure 2.12-125.

2.12.2.2.57 Engelhard Gold A-1560 (5C) fired over EMCA dielectric 3186C (9D), Figure 2.12-126.

2.12.2.2.58 Engelhard Gold A-1560 (5C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-127.

2.12.2.2.59 Engelhard Gold A-1560 (5C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-128.

2.12.2.2.60 Engelhard Gold A-1560 (5C) fired over Electro Oxide Corporation dielectric 6208 (12D). Figure 2.12-129.

2.12.2.2.61 DuPont Gold 9260 (6C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-130.

2.12.2.2.62 DuPont Gold 9260 (6C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-131.

2.12.2.2.63 DuPont Gold 9260 (6C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-132.

2.12.2.2.64 DuPont Gold 9260 (6C) fired over DuPont dielectric 8299 (4D), Figure 2.12-133.

2.12.2.2.65 DuPont Gold 9260 (6C) fired over DuPont dielectric 9429 (5D), Figure 2.12-134.

2.12.2.2.66 DuPont Gold 9260 (6C) fired over Electro Science Corporation dielectric 6408C (6D), Figure 2.12-135

2.12.2.2.67 DuPont Gold 9260 (6C) fired over Electro Science Corporation dielectric 6408 CFB-M2 (7D), Figure 2.12-136.

2.12.2.2.68 DuPont Gold 9260 (6C) fired over EMCA dielectric 3186B (8D), Figure 2.12-137.

2.12.2.2.69 DuPont Gold 9260 (6C) fired over EMCA dielectric 3186C, (9D), Figure 2.12-138.

2.12.2.2.70 DuPont Gold 9260 (6C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-139.

2.12.2.2.70 DuPont Gold 9260 (6C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-140.

2.12.2.2.71 DuPont Gold 9260 (6C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-141.

2.12.2.2.72 DuPont Gold 8237 (7C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-142.

2.12.2.2.73 DuPont Gold 8237 (7C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-143.

2.12.2.2.74 DuPont Gold 8237 (7C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-144.

2.12.2.2.75 DuPont Gold 8237 (7C) fired over DuPont dielectric 8299 (4D), Figure 2.12-145.

2.12.2.2.76 DuPont Gold 8237 (7C) fired over DuPont dielectric 9429 (5D) Figure 2.12-146.

2.12.2.2.77 DuPont Gold 8237 (7C) fired over Electro Science Corporation dielectric 6408C (6D), Figure 2.12-147.

2.12.2.2.78 DuPont Gold 8237 (7C) fired over Electro Science Corporation dielectric 6408 CFB-M2 (7D), Figure 2.12-148.

2.12.2.2.79 DuPont Gold 8237 (7C) fired over EMCA dielectric 3186B (8D), Figure 2.12-149.

2.12.2.2.80 DuPont Gold 8237 (7C) fired over EMCA dielectric 3186C (9D), Figure 2.12-150.

2.12.2.2.81 DuPont Gold 8237 (7C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-151.

2.12.2.2.82 DuPont Gold 8237 (7C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-152.

2.12.2.2.83 DuPont Gold 8237 (7C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-153.

2.12.2.2.84 Electro Science Gold 8835-1B (8C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-154.

2.12.2.2.85 Electro Science Gold 8835-1B (8C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-155.

2.12.2.2.86 Electro Science Gold 8835-1B (8C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-156.

2.12.2.2.87 Electro Science Gold 8835-1B (8C) fired over DuPont dielectric 8299 (4D), Figure 2.12-157.

2.12.2.2.88 Electro Science Gold 8835-1B (8C) fired over DuPont dielectric 9429 (5D), Figure 2.12-158.

2.12.2.2.89 Electro Science Gold 8835-1B (8C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-159.

2.12.2.2.90 Electro Science Gold 8835-1B (8C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-160.

2.12.2.2.91 Electro Science Gold 8835-1B (8C) fired over EMCA dielectric 3186B (8D), Figure 2.12-161.

2.12.2.2.92 Electro Science Gold 8835-1B (8C) fired over EMCA dielectric 3186C (9D), Figure 2.12-162.

2.12.2.2.93 Electro Science Gold 8835-1B (8C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-163.

2.12.2.2.94 Electro Science Gold 8835-1B (8C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-164.

2.12.2.2.95 Electro Science Gold 8835-1B (8C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-165.

2.12.2.2.96 Electro Science Gold 8835 (9C) fired over Thick Film Systems dielectric 1017 RCA (1D) Figure 2.12-166.

2.12.2.2.97 Electro Science Gold 8835 (9C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-167.

2.12.2.2.98 Electro Science Gold 8835 (9C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-168.

2.12.2.2.99 Electro Science Gold 8835 (9C) fired over DuPont dielectric 8299 (4D), Figure 2.12-169.

2.12.2.2.100 Electro Science Gold 8835 (9C) fired over DuPont dielectric 9429 (5D), Figure 2.12-170.

2.12.2.2.101 Electro Science Gold 8835 (9C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-171.

2.12.2.2.102 Electro Science Gold 8835 (9C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-172.

2.12.2.2.103 Electro Science Gold 8835 (9C) fired over EMCA dielectric 3186B (8D), Figure 2.12-173.

2.12.2.2.104 Electro Science Gold 8835 (9C) fired over EMCA dielectric 3186C (9D), Figure 2.12-174.

2.12.2.2.105 Electro Science Gold 8835 (9C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-175.

2.12.2.2.106 Electro Science Gold 8835 (9C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-176.

2.12.2.2.107 Electro Science Gold 8835 (9C) fired over Electro Oxide dielectric 6208 (12D), Figure 2.12-177.

2.12.2.2.108 EMCA Gold EXK3264 (10C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-178.

2.12.2.2.109 EMCA Gold EXK3264 (10C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-179.

2.12.2.2.110 EMCA Gold EXK3264 (10C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-180.

2.12.2.2.111 EMCA Gold EXK3264 (10C) fired over DuPont dielectric 8299 (4D), Figure 2.12-181.

2.12.2.2.112 EMCA Gold EXK3264 (10C) fired over DuPont dielectric 9429 (5D), Figure 2.12-182.

2.12.2.2.113 EMCA Gold EXK3264 (10C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-183.

2.12.2.2.114 EMCA Gold EXK3264 (10C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-184.

2.12.2.2.115 EMCA Gold EXK3264 (10C) fired over EMCA dielectric 3186B (8D), Figure 2.12-185.

2.12.2.2.116 EMCA Gold EXK3264 (10C) fired over EMCA dielectric 3186C (9D), Figure 2.12-186.

2.12.2.2.117 EMCA Gold EXK3264 (10C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-187.

2.12.2.2.118 EMCA Gold EXK3264 (10C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-188.

2.12.2.2.119 EMCA Gold EXK3264 (10C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-189.

2.12.2 2.120 DuPont Gold 8653 (11C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-190.

2.12.2.2.121 DuPont Gold 8653 (11C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-191.

2.12.2.2.122 DuPont Gold 8653 (11C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-192.

2.12.2.2.123 DuPont Gold 8653 (11C) fired over DuPont dielectric 8299 (4D), Figure 2.12-193.

2.12.2.2.124 DuPont Gold 8653 (11C) fired over DuPont dielectric 9429 (5D), Figure 2.12-194.

2.12.2.2.125 DuPont Gold 8653 (11C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-195.

2.12.2.2.126 DuPont Gold 8653 (11C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-196.

2.12.2.2.127 DuPont Gold 8653 (11C) fired over EMCA dielectric 3186B (8D), Figure 2.12-197.

2.12.2.2.128 DuPont Gold 8653 (11C) fired over EMCA dielectric 3186C (9D), Figure 2.12-198.

2.12.2.2.129 DuPont Gold 8653 (11C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-199.

2.12.2.2.130 DuPont Gold 8653 (11C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-200.

2.12.2.2.131 DuPont Gold 8653 (11C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-201.

2.12.2.2.132 EMCA Gold EXK3283 (12C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-202.

2.12.2.2.133 EMCA Gold EXK3283 (12C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-203.

2.12.2.2.134 EMCA Gold EXK3283 (12C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-204.

2.12.2.2.135 EMCA Gold EXK3283 (12C) fired over DuPont dielectric 8299 (4D), Figure 2.12-205.

2.12.2.2.136 EMCA Gold EXK3283 (12C) fired over DuPont dielectric 9429 (5D), Figure 2.12-206.

2.12.2.2.137 EMCA Gold EXK3283 (12C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-207.

2.12.2.2.138 EMCA Gold EXK3283 (12C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-208.

2.12.2.2.139 EMCA Gold EXK3283 (12C) fired over EMCA dielectric 3186B (8D), Figure 2.12-209.

2.12.2.2.140 EMCA Gold EXK3283 (12C) fired over EMCA dielectric 3186C (9D), Figure 2.12-210.

2.12.2.2.141 EMCA Gold EXK3283 (12C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-211.

2.12.2.2.142 EMCA Gold EXK3283 (12C) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-212.

2.12.2.2.143 EMCA Gold EXK3283 (12C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-213.

2.12.2.2.144 Sel-Rex Company Gold DX-799 (13C) fired over Thick Film Systems dielectric 1017 RCA (1D). Figure 2.12-214.

2.12.2.2.145 Sel-Rex Company Gold DX-799 (13C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-215.

2.12.2.2.146 Sel-Rex Company Gold DX-799 (13C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-216.

2.12.2.2.147 Sel-Rex Company Gold DX-799 (13C) fired over DuPont dielectric 8299 (4D), Figure 2.12-217.

2.12.2.2.148 Sel-Rex Company Gold DX-799 (13C) fired over DuPont dielectric 9429 (5D), Figure 2.12-218.

2.12.2.2.149 Sel-Rex Company Gold DX-799 (13C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-219.

2.12.2.2.150 Sel-Rex Company Gold DX-799 (13C) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-220.

2.12.2.2.151 Sel-Rex Company Gold DX-799 (13C) fired over EMCA dielectric 3186B (8D), Figure 2.12-221.

2.12.2.2.152 Sel-Rex Company Gold DX-799 (13C) fired over EMCA dielectric 3186C (9D), Figure 2.12-222.

2.12.2.2.153 Sel-Rex Company Gold DX-799 (13C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-223.

2.12.2.2.154 Sel-Rex Company Gold DX-799 (13C) fired over Thick Film Systems dielectric 1017 RCY (11D). Figure 2.12-224.

2.12.2.2.155 Sel-Rex Company Gold DX-799 (13C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-225.

2.12.2.2.156 Electro Oxide Corporation Gold 6990 (14C) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-226.

2.12.2.2.157 Electro Oxide Corporation Gold 6990 (14C) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-227.

2.12.2.2.158 Electro Oxide Corporation Gold 6990 (14C) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-228.

2.12.2.2.159 Electro Oxide Corporation Gold 6990 (14C) fired over DuPont dielectric 8299 (4D), Figure 2.12-229.

2.12.2.2.160 Electro Oxide Corporation Gold 6990 (14C) fired over DuPont dielectric 9429 (5D), Figure 2.12-230.

2.12.2.2.161 Electro Oxide Corporation Gold 6990 (14C) fired over Electro Science dielectric 6408C (6D), Figure 2.12-231.

2.12.2.2.162 Electro Oxide Corporation Gold 6990 (14C) fired over Electro Science dielectric 6408 CFB-M-2 (7D) Figure 2.12-232.

2.12.2.2.163 Electro Oxide Corporation Gold 6990 (14C) fired over EMCA dielectric 3186B (8D), Figure 2.12-233.

2.12.2.2.164 Electro Oxide Corporation Gold 6990 (14C) fired over EMCA dielectric 3186C (9D), Figure 2.12-234.

2.12.2.2.165 Electro Oxide Corporation Gold 6990 (14C) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-235.

2.12.2.2.166 Electro Oxide Corporation Gold 6990 (14C) fired over Thick Film Systems dielectric 1017 RCY (11D). Figure 2.12-236.

2.12.2.2.167 Electro Oxide Corporation Gold 6990 (14C) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-237.

2.12.2.2.168 Engelhard Nickel A-2884 (2SC) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-238.

2.12.2.2.169 Engelhard Nickel A-2884 (2SC) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-239.

2.12.2.2.170 Engelhard Nickel A-2884 (2SC) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-240.

2.12.2.2.171 Engelhard Nickel A-2884 (2SC) fired over DuPont dielectric 8299 (4D), Figure 2.12-241.

2.12.2.2.172 Engelhard Nickel A-2884 (2SC) fired over DuPont dielectric 9429 (5D), Figure 2.12-242.

2.12.2.2.173 Engelhard Nickel A-2884 (2SC) fired over Electro Science dielectric 6408C (6D), Figure 2.12-243.

2.12.2.2.174 Engelhard Nickel A-2884 (2SC) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-244.

2.12.2.2.175 Engelhard Nickel A-2884 (2SC) fired over EMCA dielectric 3186B (8D), Figure 2.12-245.

2.12.2.2.176 Engelhard Nickel A-2884 (2SC) fired over EMCA dielectric 3186C (9D) Figure 2.12-246.

2.12.2.2.177 Engelhard Nickel A-2884 (2SC) fired over EMCA dielectric EXK3274 (10D) Figure 2.12-247.

2.12.2.2.178 Engelhard Nickel A-2884 (2SC) fired over Thick Film Systems dielectric 1017 RCY (11D), Figure 2.12-248.

2.12.2.2.179 Engelhard Nickel A-2884 (2SC) fired over Electro Oxide Corporation dielectric 6208 (12D) Figure 2.12-249.

2.12.2.2.180 Engelhard Aluminum A-2746 (3SC) fired over Thick Film Systems dielectric 1017 RCA (1D), Figure 2.12-250.

2.12.2.2.181 Engelhard Aluminum A-2746 (3SC) fired over Thick Film Systems dielectric 1005 TCG (2D), Figure 2.12-251.

2.12.2.2.182 Engelhard Aluminum A-2746 (3SC) fired over Engelhard dielectric A-2835 (3D), Figure 2.12-252.

2.12.2 2.183 Engelhard Aluminum A-2746 (3SC) fired over DuPont dielectric 8299 (4D), Figure 2.12-253.

2.12.2.2.184 Engelhard Aluminum A-2746 (3SC) fired over DuPont dielectric 9429 (5D), Figure 2.12-254.

2.12.2.2.185 Engelhard Aluminum A-2746 (3SC) fired over Electro Science dielectric 6408C (6D), Figure 2.12-255.

2.12 2.2.186 Engelhard Aluminum A-2746 (3SC) fired over Electro Science dielectric 6408 CFB-M2 (7D), Figure 2.12-256.

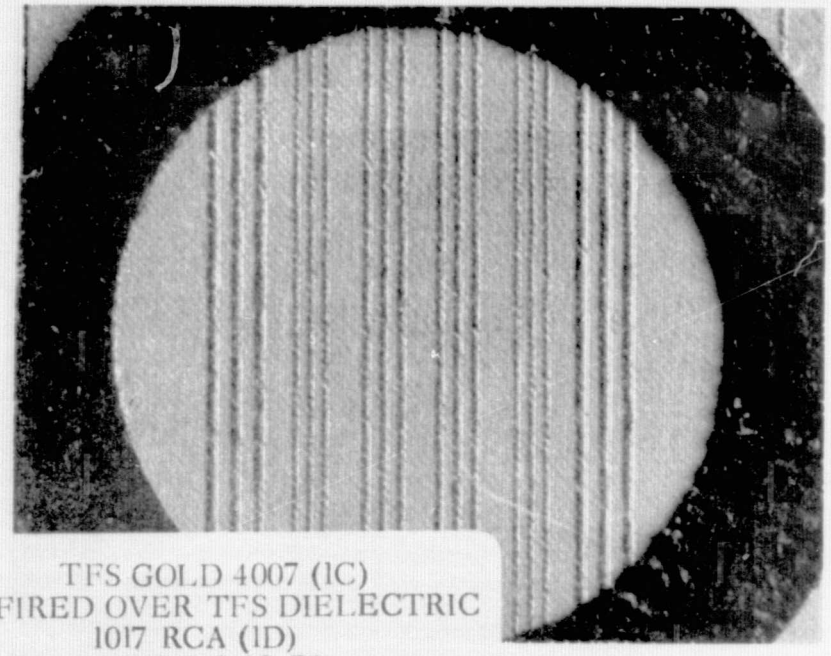
2.12.2.2.187 Engelhard Aluminum A-2746 (3SC) fired over EMCA dielectric 3186B (8D), Figure 2.12-257.

2.12.2.2.188 Engelhard Aluminum A-2746 (3SC) fired over EMCA dielectric 3186C (9D), Figure 2.12-258.

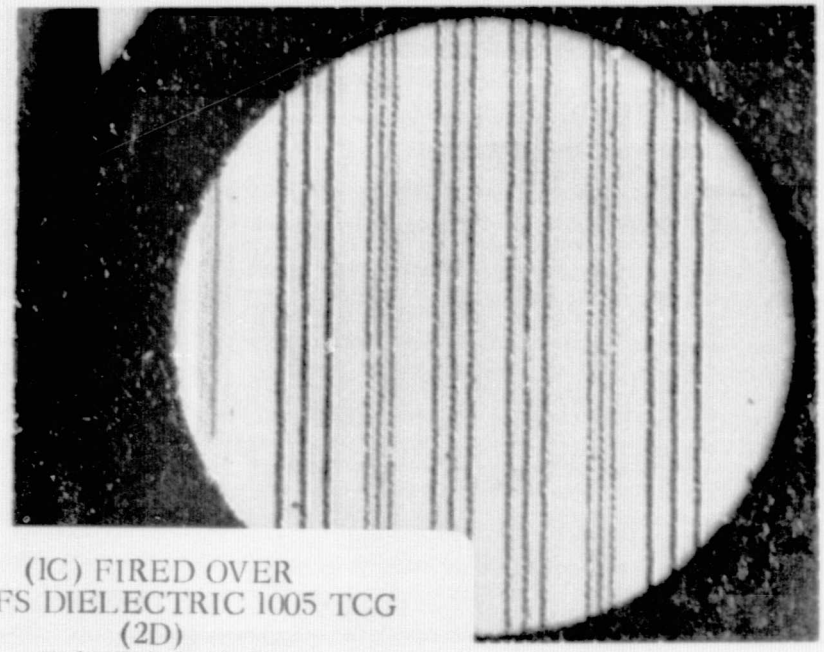
2.12.2.2.189 Engelhard Aluminum A-2746 (3SC) fired over EMCA dielectric EXK3274 (10D), Figure 2.12-259.

2.12.2.2.190 Engelhard Aluminum A-2746 (3SC) fired over Thick Film Systems dielectric 1017 RCY (11D) Figure 2.12-260.

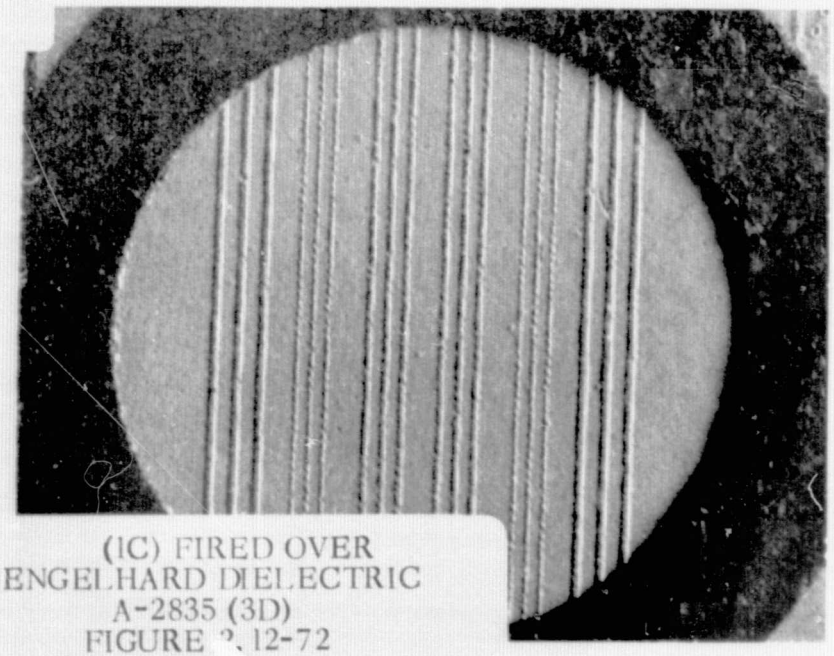
2.12.2.2.191 Engelhard Aluminum A-2746 (3SC) fired over Electro Oxide Corporation dielectric 6208 (12D), Figure 2.12-261.



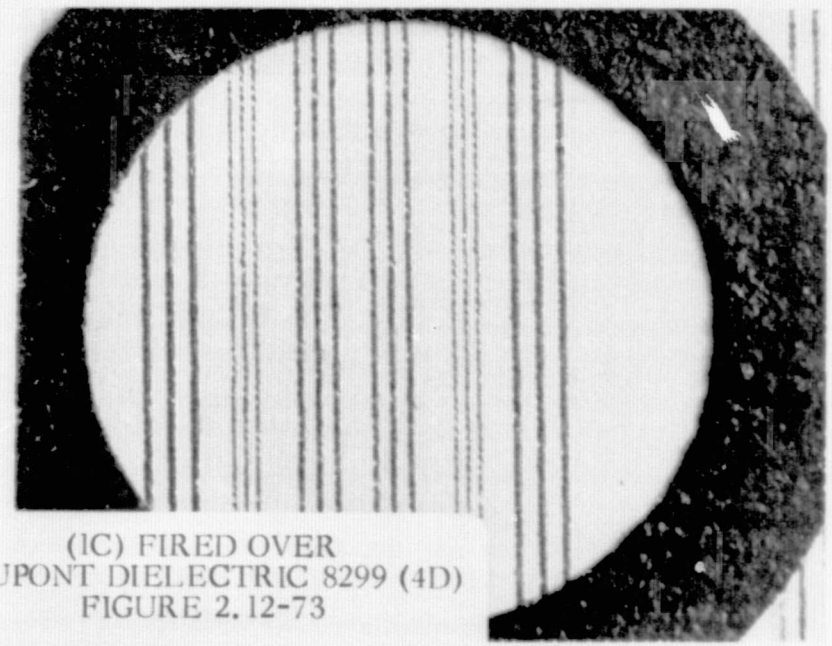
TFS GOLD 4007 (1C)
FIRED OVER TFS DIELECTRIC
1017 RCA (1D)
FIGURE 2.12-70



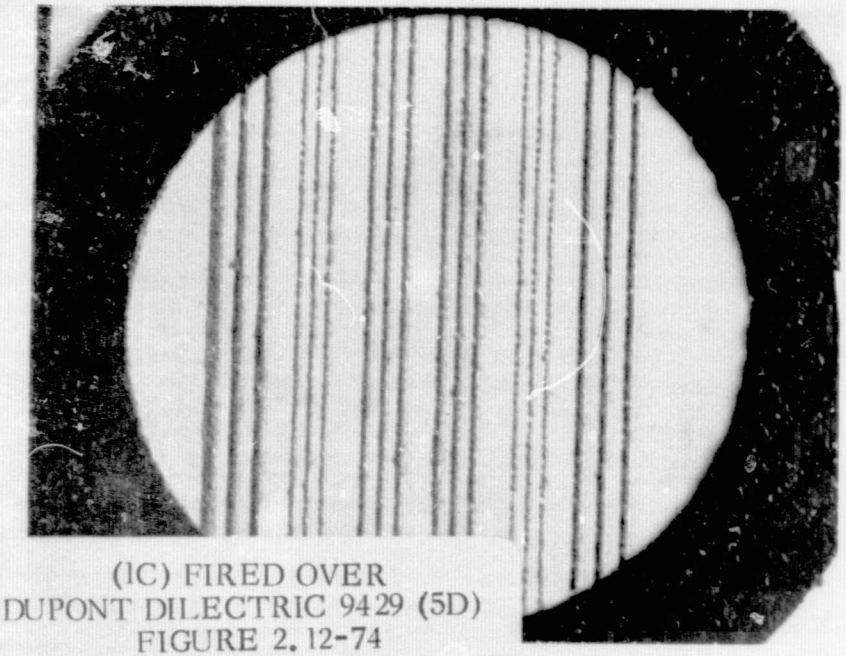
(1C) FIRED OVER
TFS DIELECTRIC 1005 TCG
(2D)
FIGURE 2.12-71



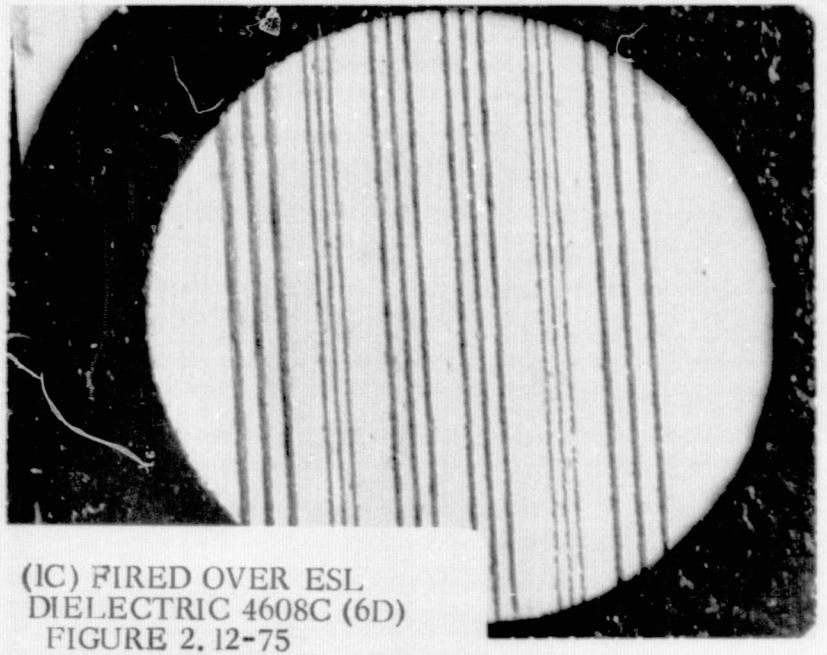
(1C) FIRED OVER
ENGELHARD DIELECTRIC
A-2835 (3D)
FIGURE 2.12-72



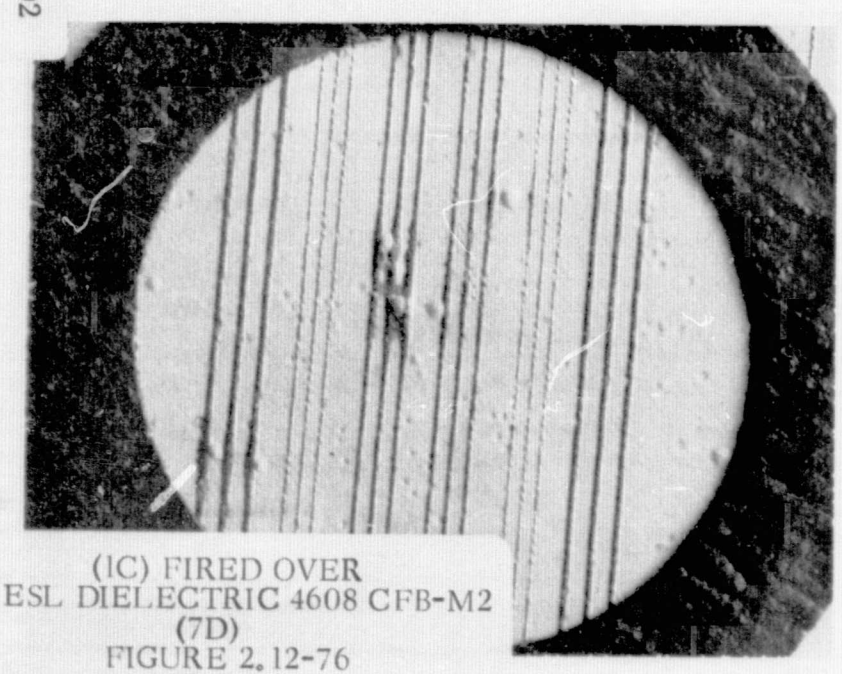
(1C) FIRED OVER
DUPONT DIELECTRIC 8299 (4D)
FIGURE 2.12-73



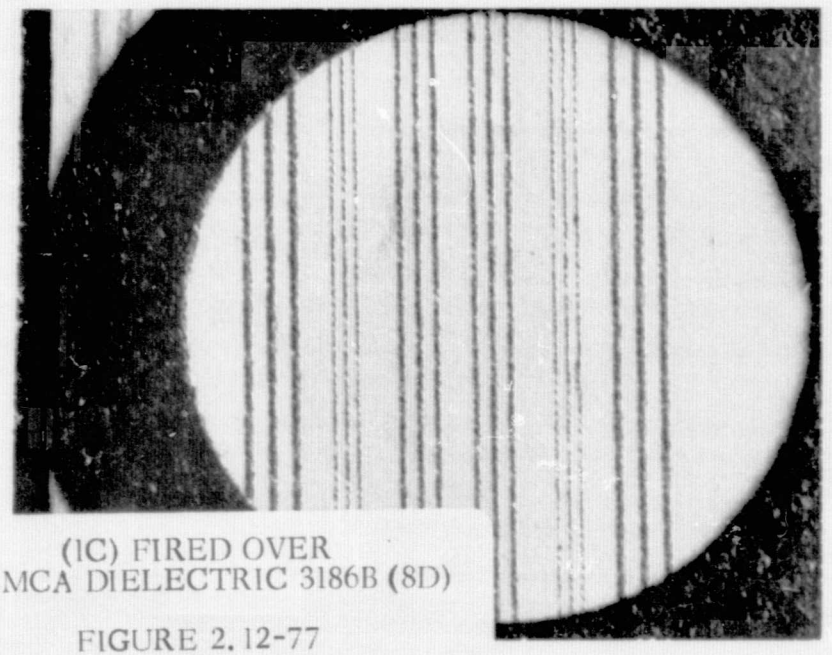
(1C) FIRED OVER
DUPONT DILECTRIC 9429 (5D)
FIGURE 2.12-74



(1C) FIRED OVER ESL
DIELECTRIC 4608C (6D)
FIGURE 2.12-75

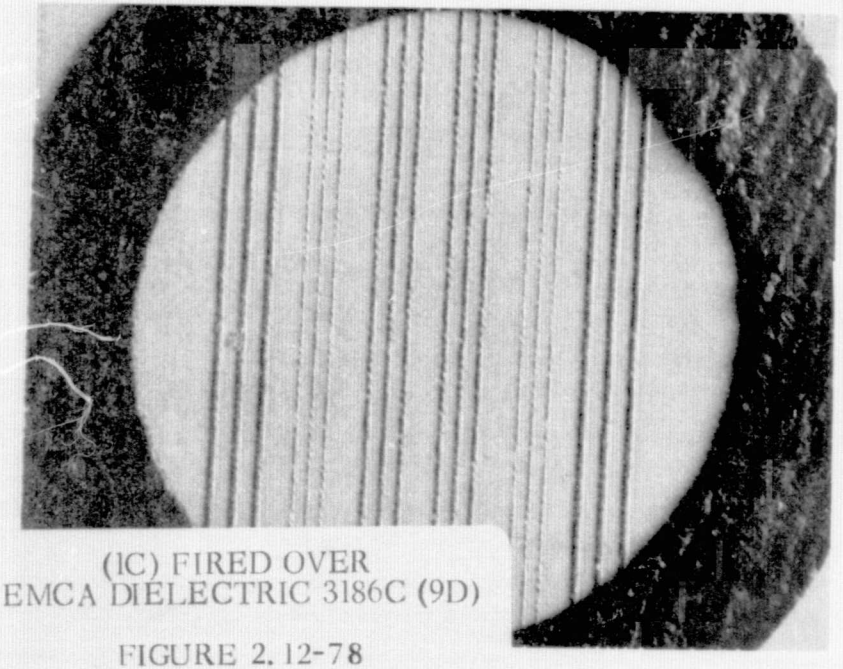


(1C) FIRED OVER
ESL DIELECTRIC 4608 CFB-M2
(7D)
FIGURE 2.12-76



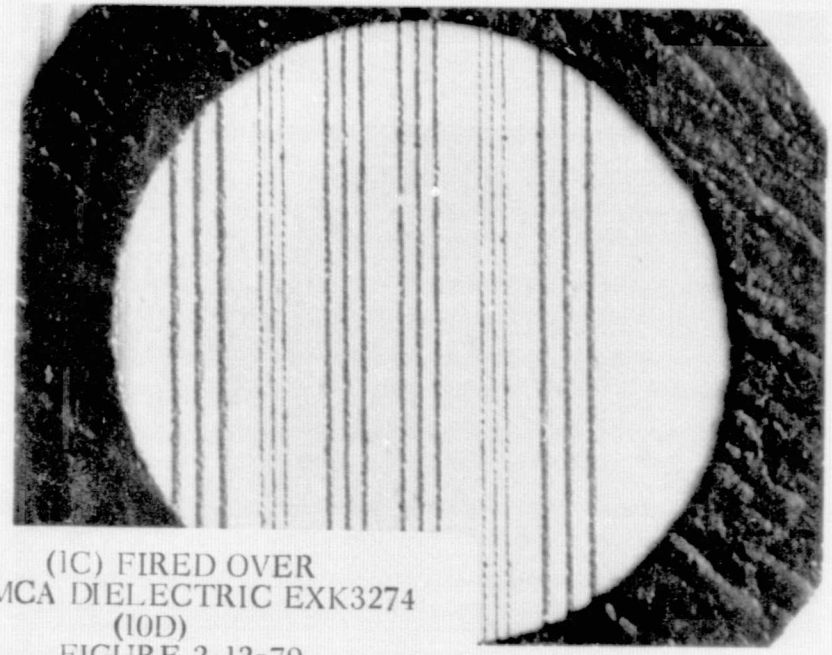
(1C) FIRED OVER
EMCA DIELECTRIC 3186B (8D)

FIGURE 2.12-77

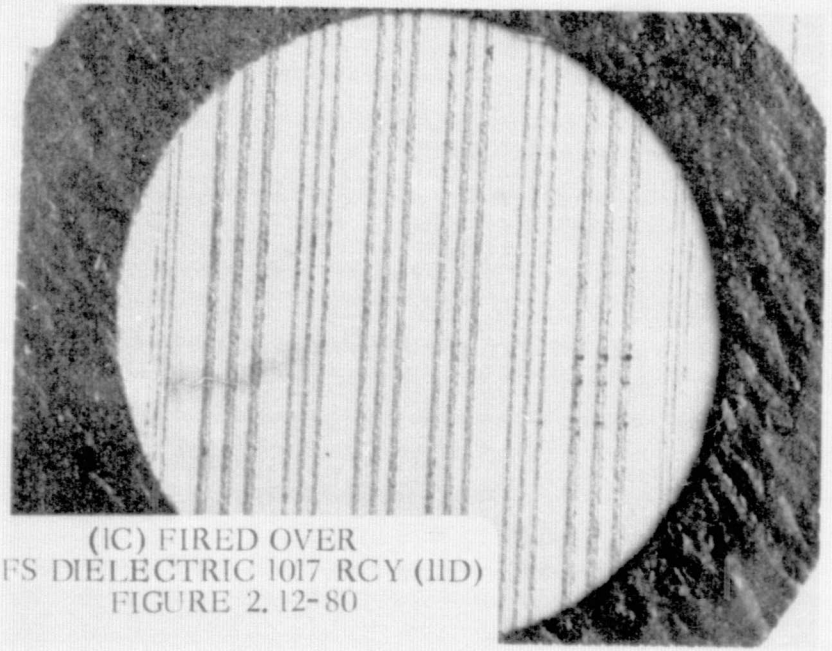


(1C) FIRED OVER
EMCA DIELECTRIC 3186C (9D)

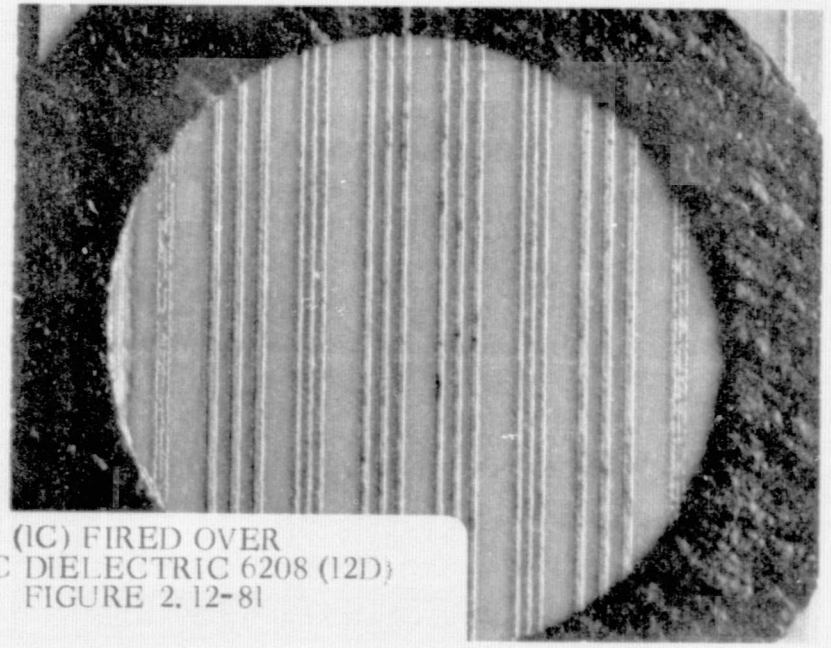
FIGURE 2.12-78



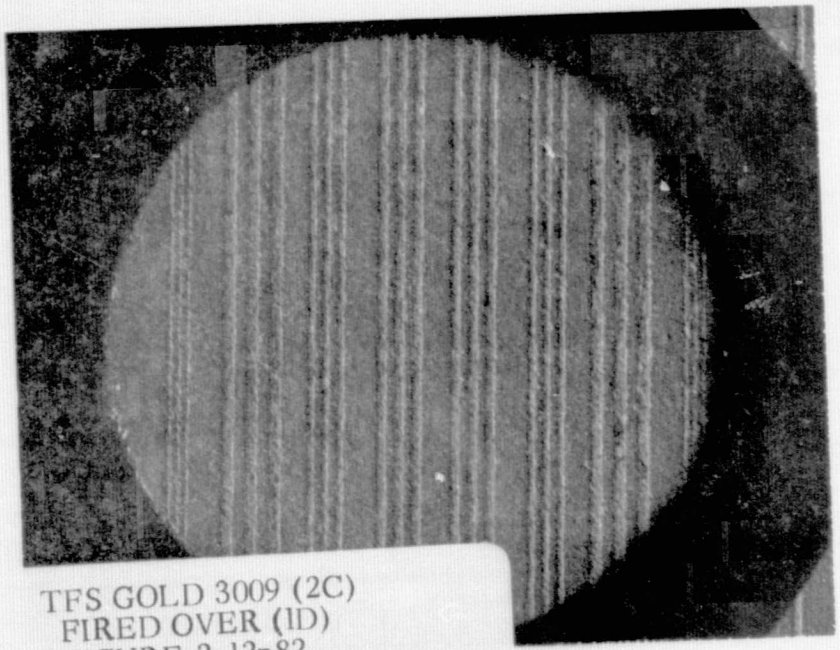
(1C) FIRED OVER
EMCA DIELECTRIC EXK3274
(10D)
FIGURE 2.12-79



(1C) FIRED OVER
TFS DIELECTRIC 1017 RCY (11D)
FIGURE 2.12-80



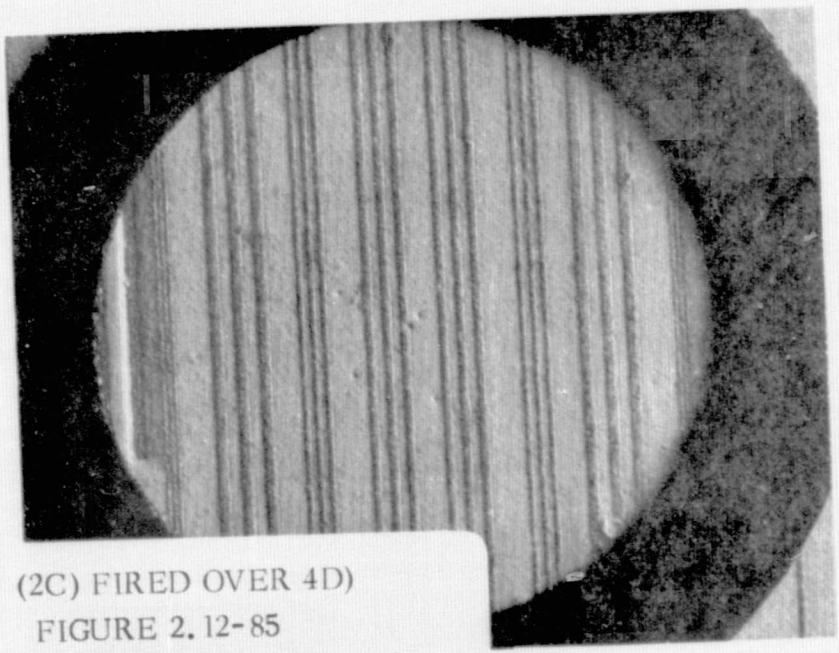
(1C) FIRED OVER
EOC DIELECTRIC 6208 (12D)
FIGURE 2.12-81



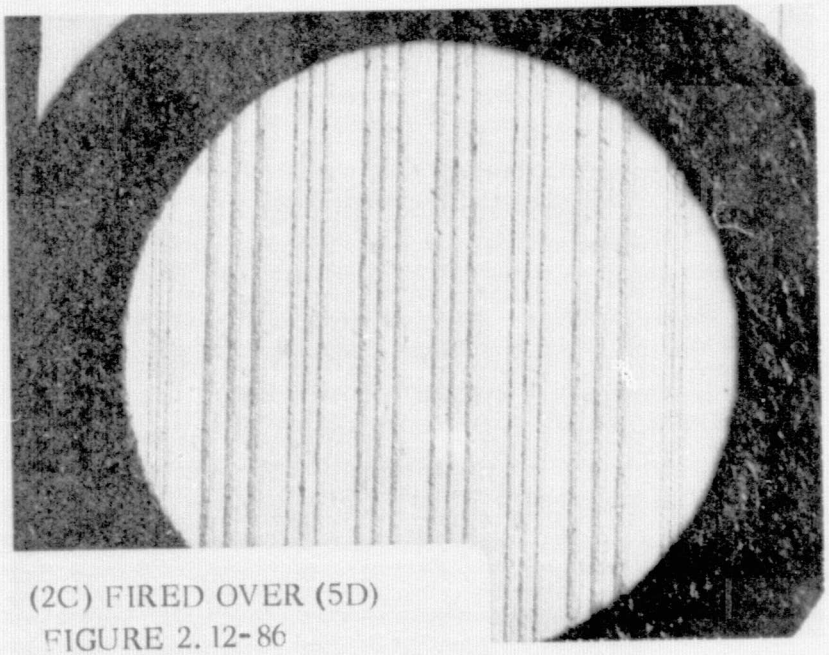
TFS GOLD 3009 (2C)
FIRED OVER (1D)
FIGURE 2.12-82

(2C) FIRED OVER (2D)
FIGURE 2.12-83

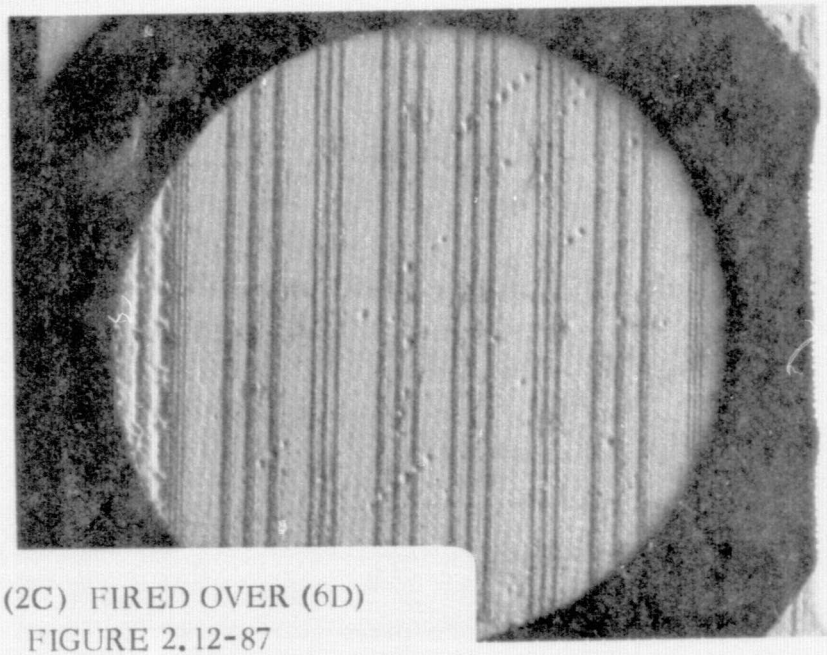
(2C) FIRED OVER (3D)
FIGURE 2.12-84



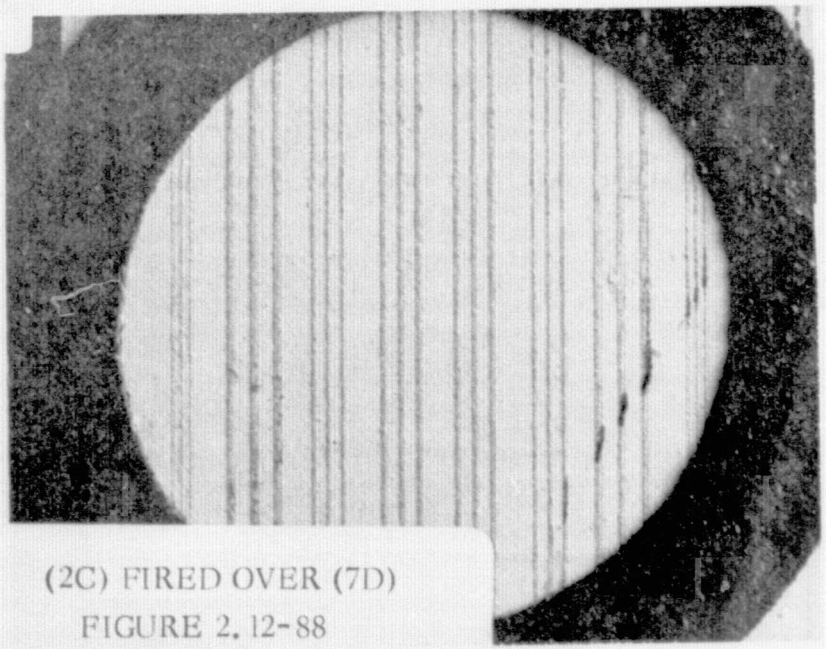
(2C) FIRED OVER 4D)
FIGURE 2.12-85



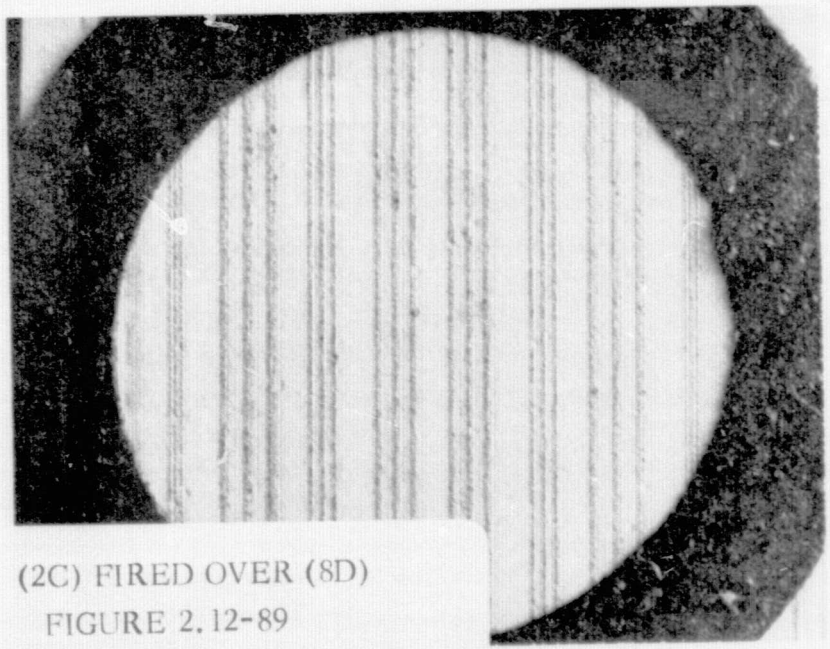
(2C) FIRED OVER (5D)
FIGURE 2.12-86



(2C) FIRED OVER (6D)
FIGURE 2.12-87

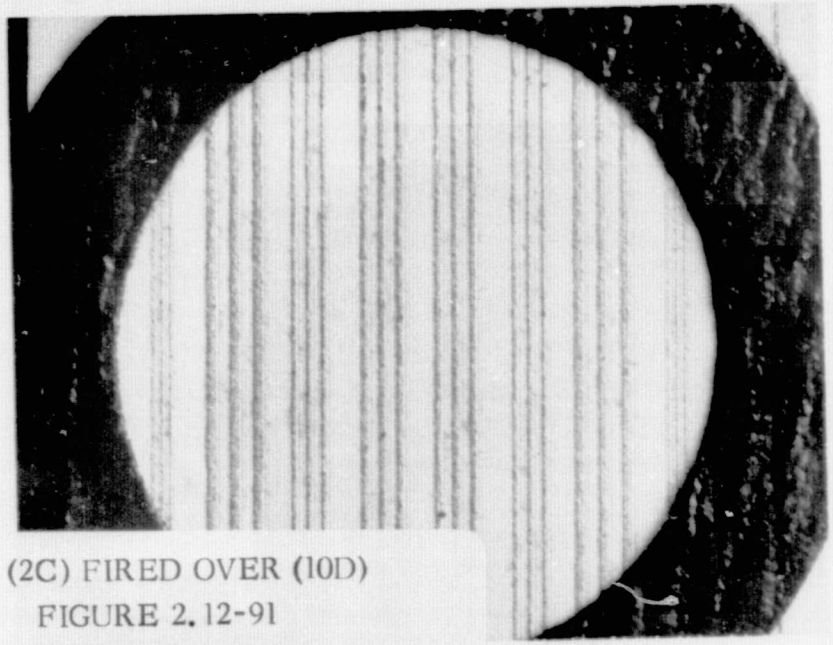


(2C) FIRED OVER (7D)
FIGURE 2.12-88

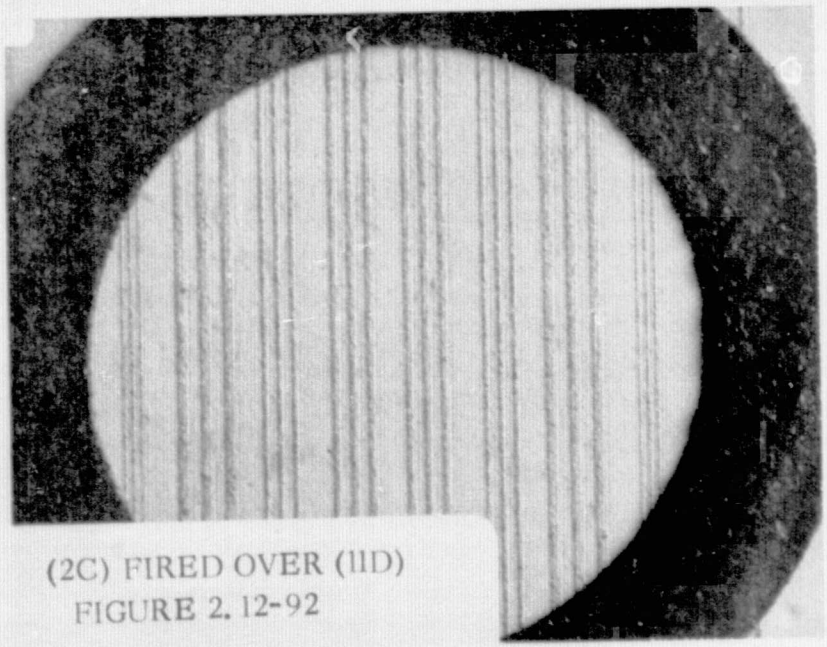


(2C) FIRED OVER (8D)
FIGURE 2.12-89

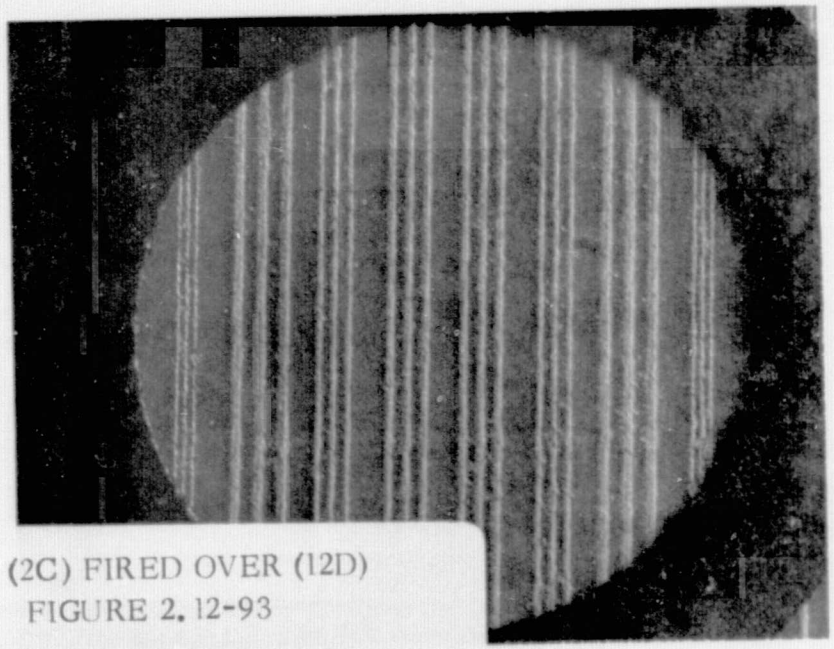
(2C) FIRED OVER (9D)
FIGURE 2.12-90



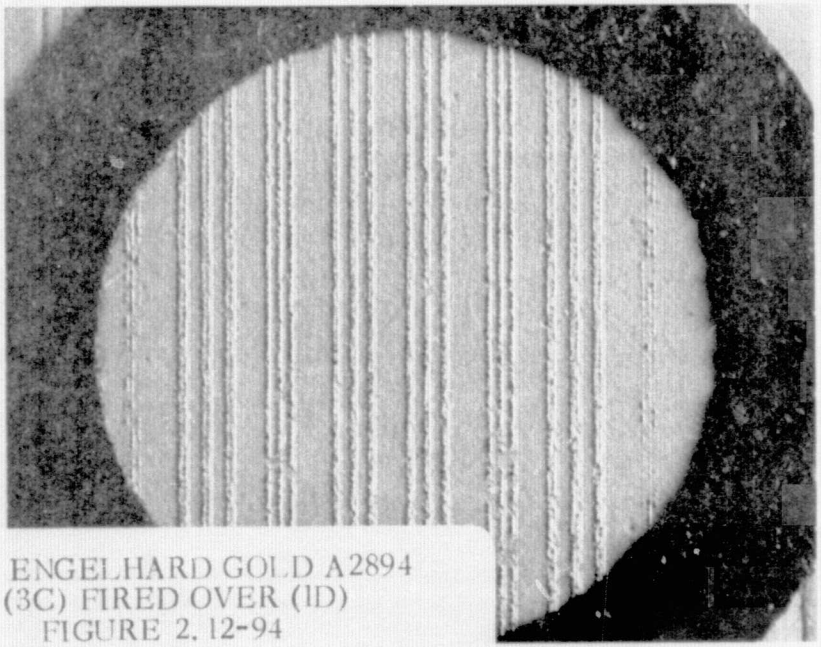
(2C) FIRED OVER (10D)
FIGURE 2.12-91



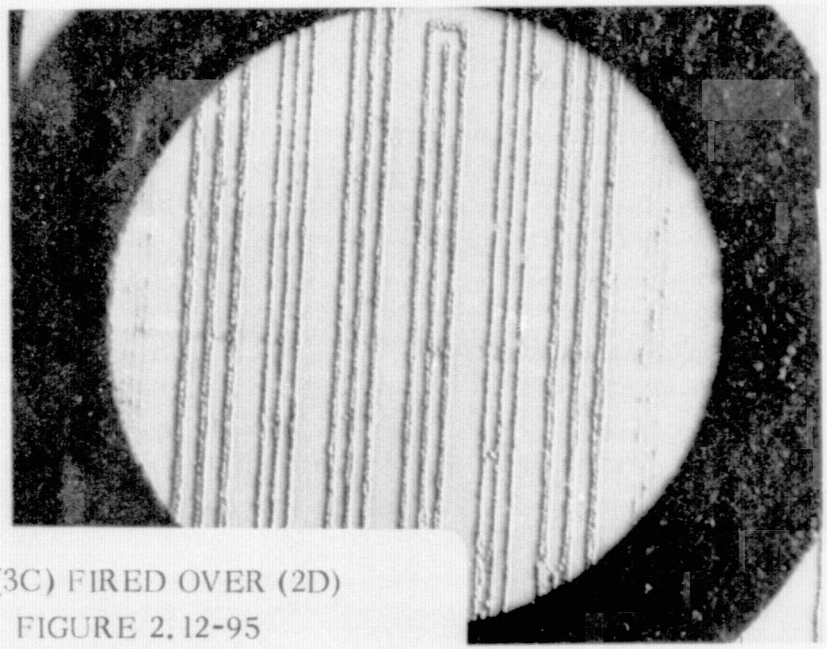
(2C) FIRED OVER (11D)
FIGURE 2.12-92



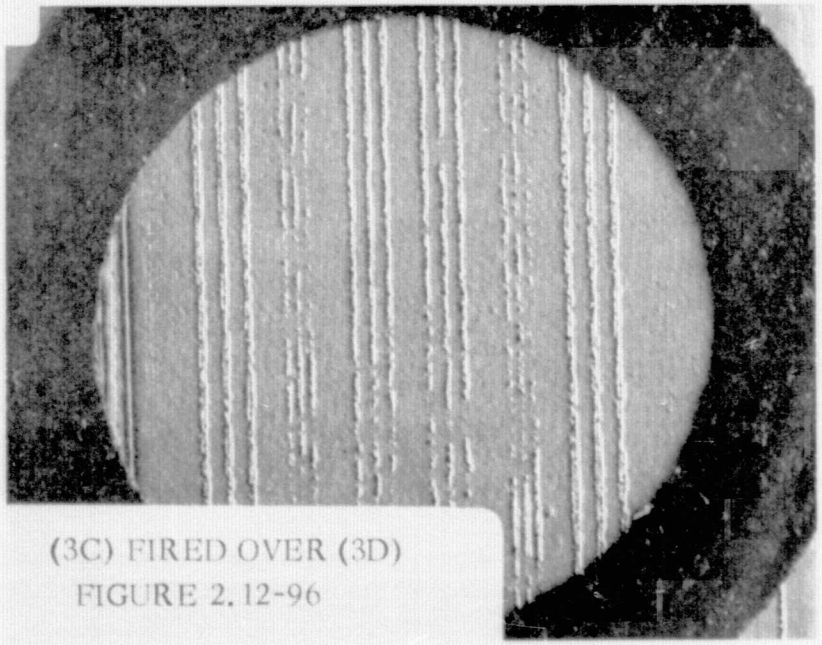
(2C) FIRED OVER (12D)
FIGURE 2.12-93



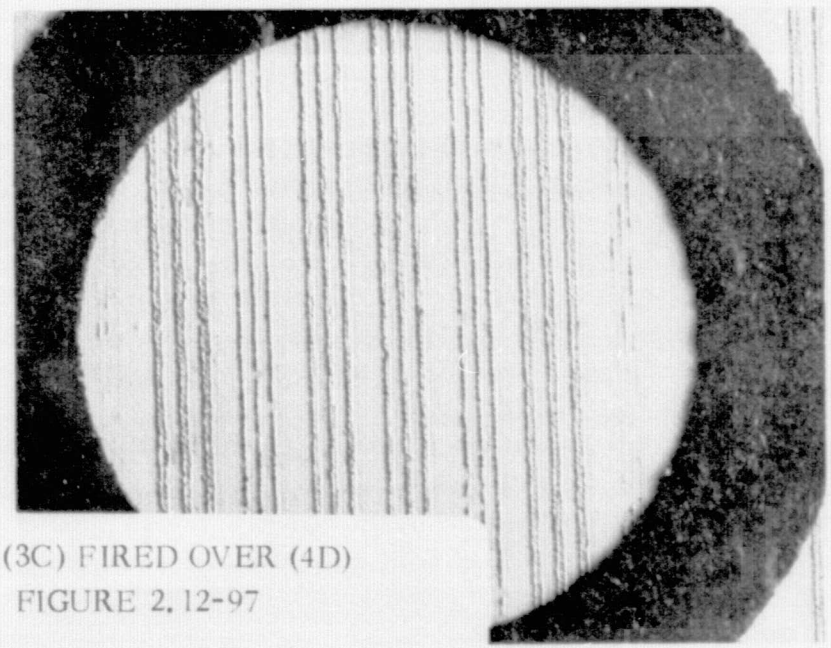
ENGELHARD GOLD A2894
(3C) FIRED OVER (1D)
FIGURE 2.12-94



(3C) FIRED OVER (2D)
FIGURE 2.12-95

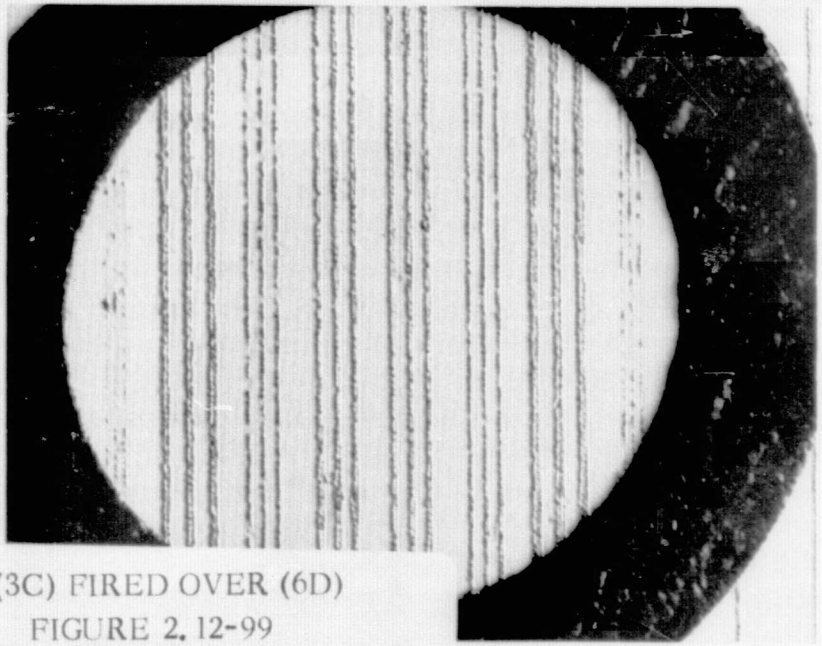


(3C) FIRED OVER (3D)
FIGURE 2.12-96

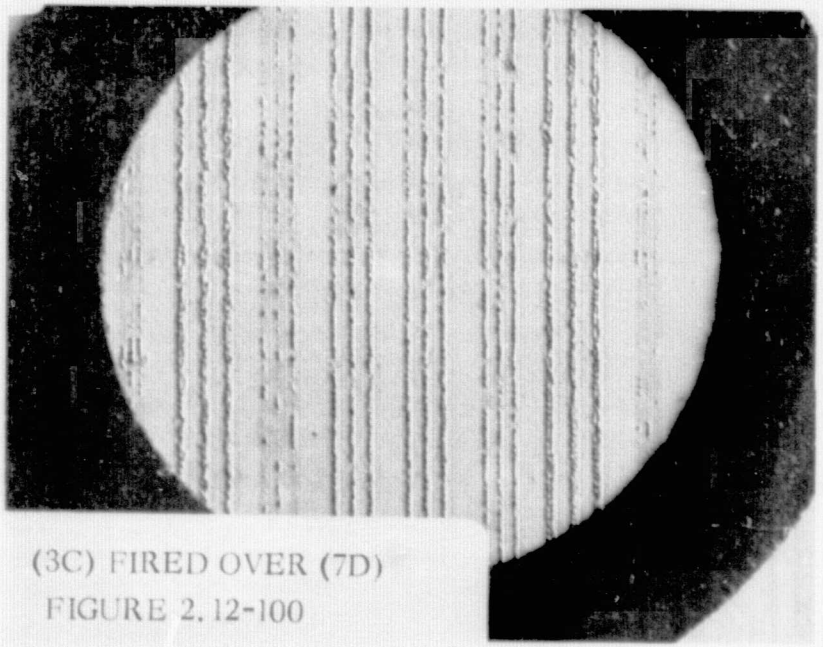


(3C) FIRED OVER (4D)
FIGURE 2.12-97

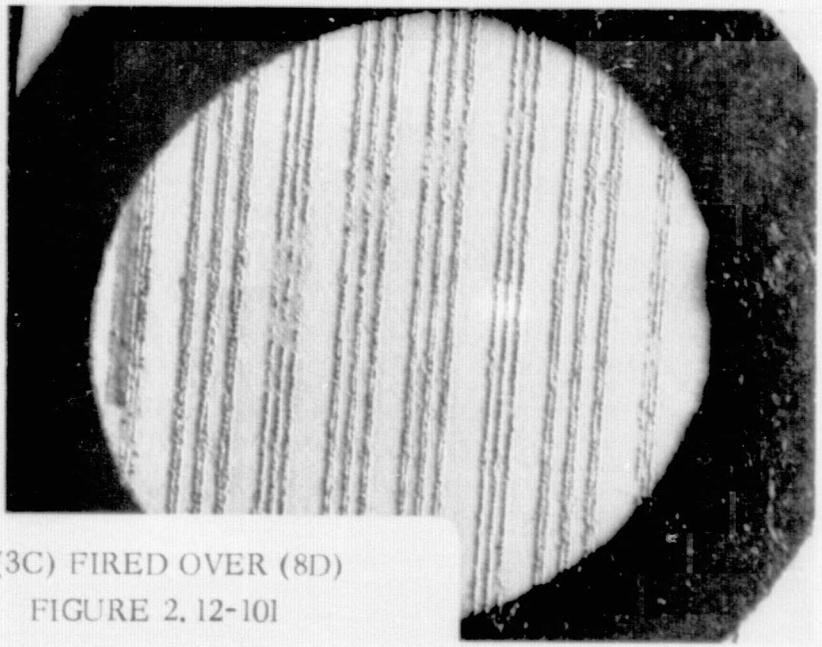
(3C) FIRED OVER (5D)
FIGURE 2.12-98



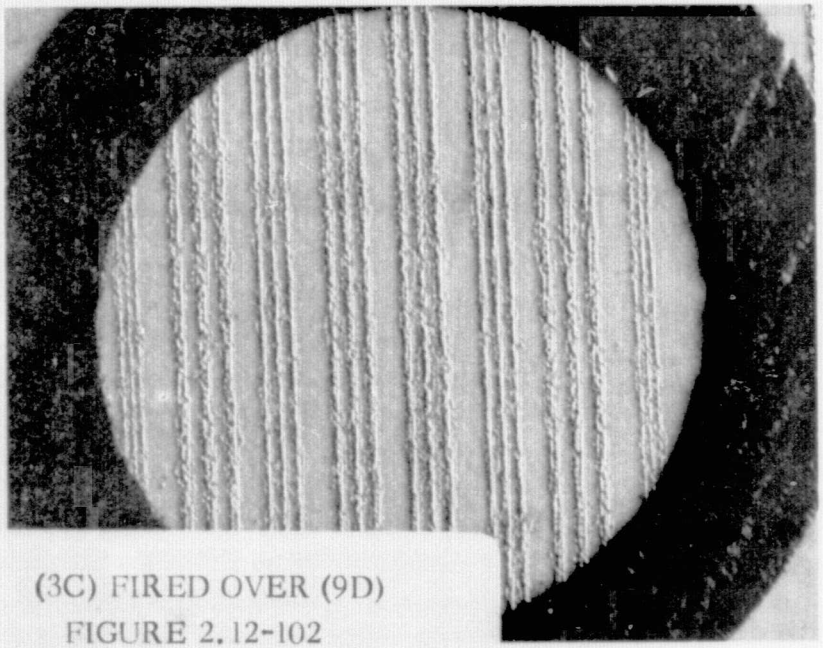
(3C) FIRED OVER (6D)
FIGURE 2.12-99



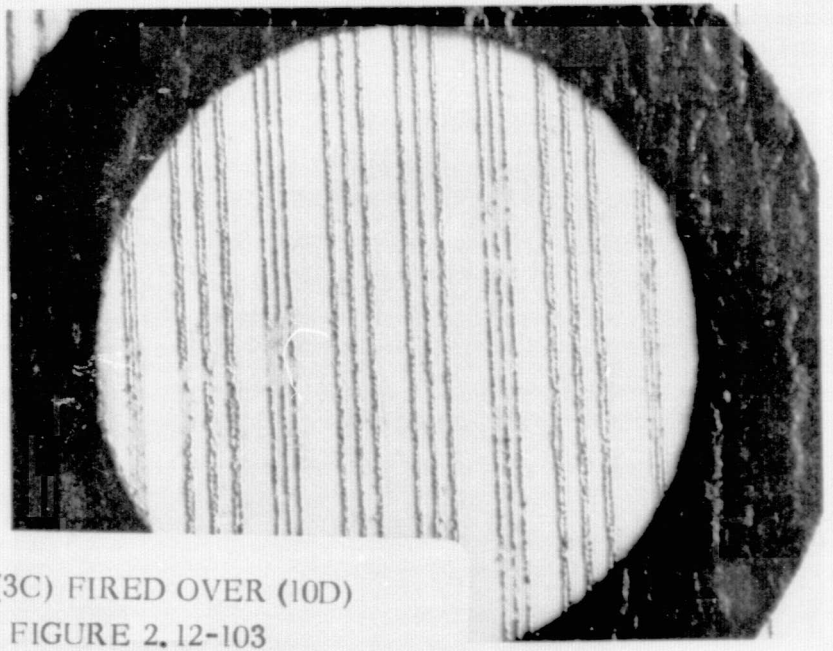
(3C) FIRED OVER (7D)
FIGURE 2.12-100



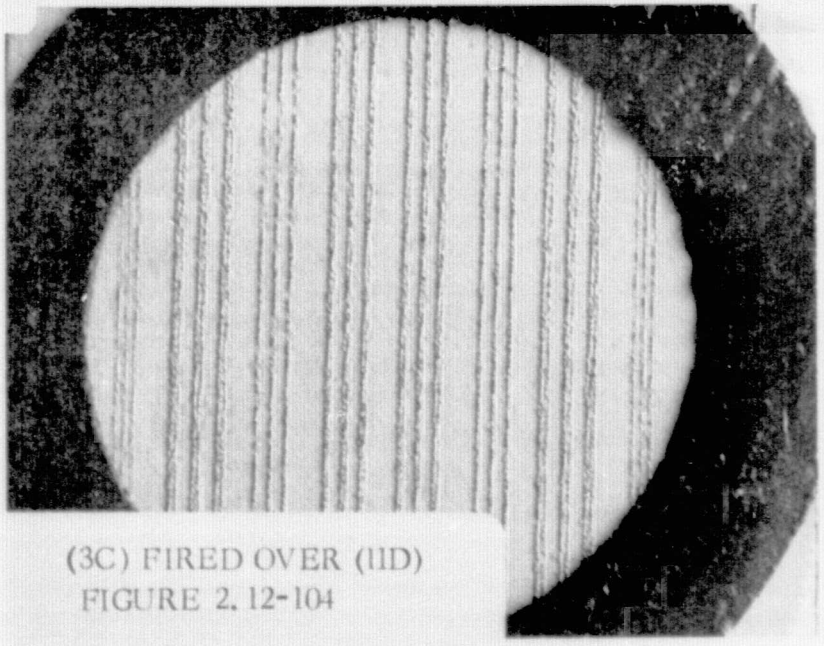
(3C) FIRED OVER (8D)
FIGURE 2.12-101



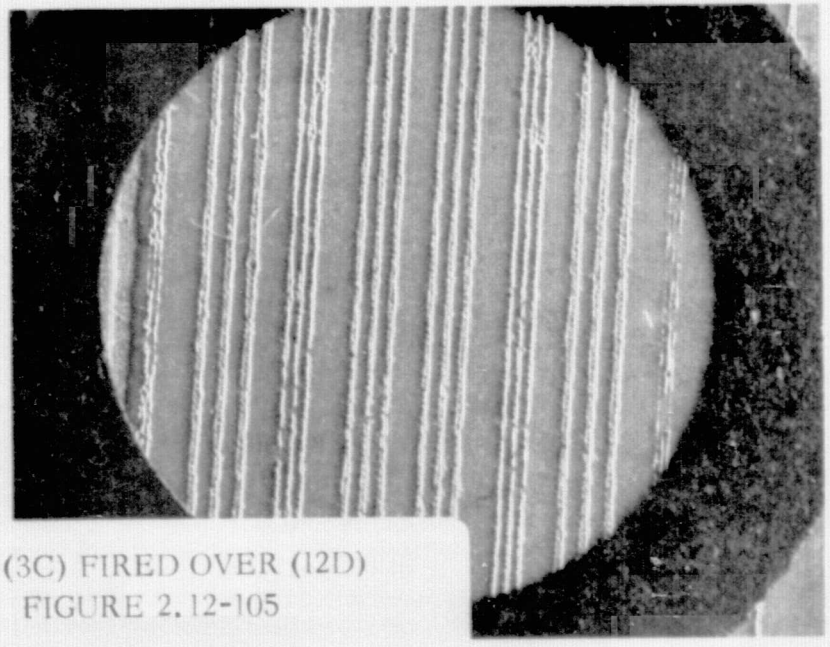
(3C) FIRED OVER (9D)
FIGURE 2.12-102



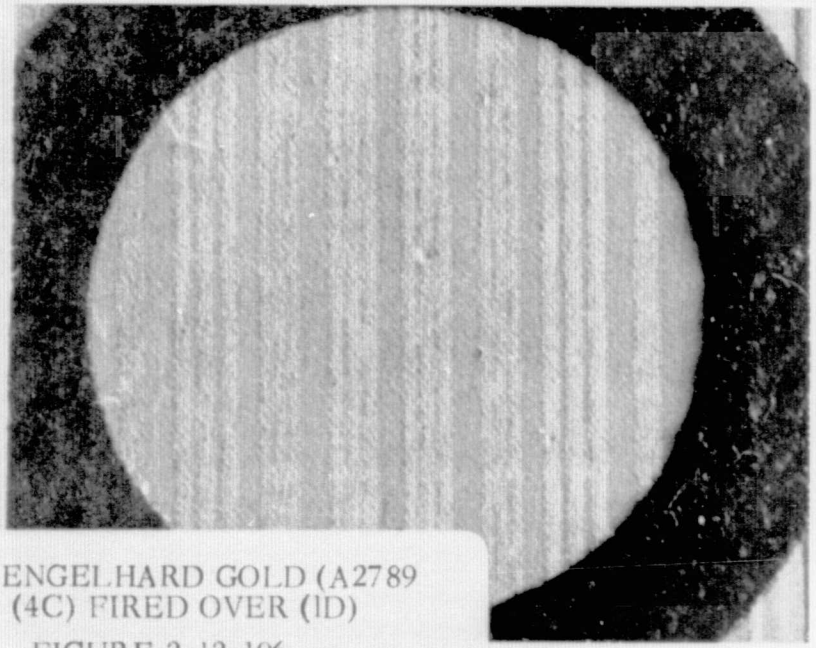
(3C) FIRED OVER (10D)
FIGURE 2.12-103



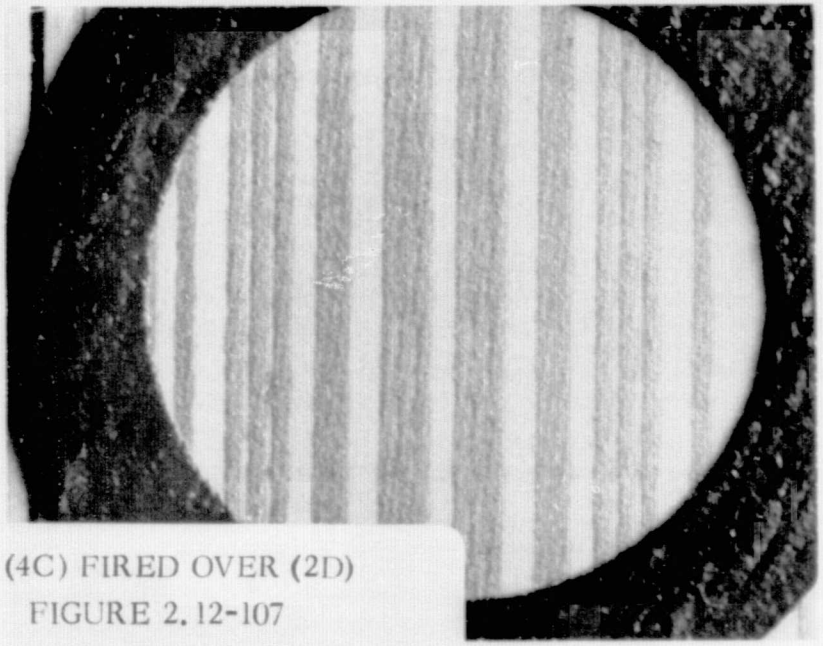
(3C) FIRED OVER (11D)
FIGURE 2.12-104



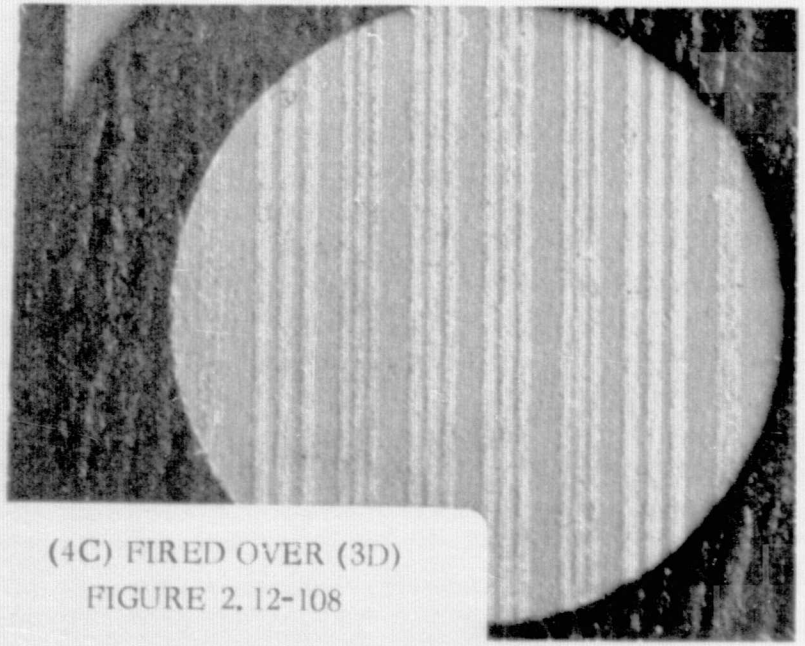
(3C) FIRED OVER (12D)
FIGURE 2.12-105



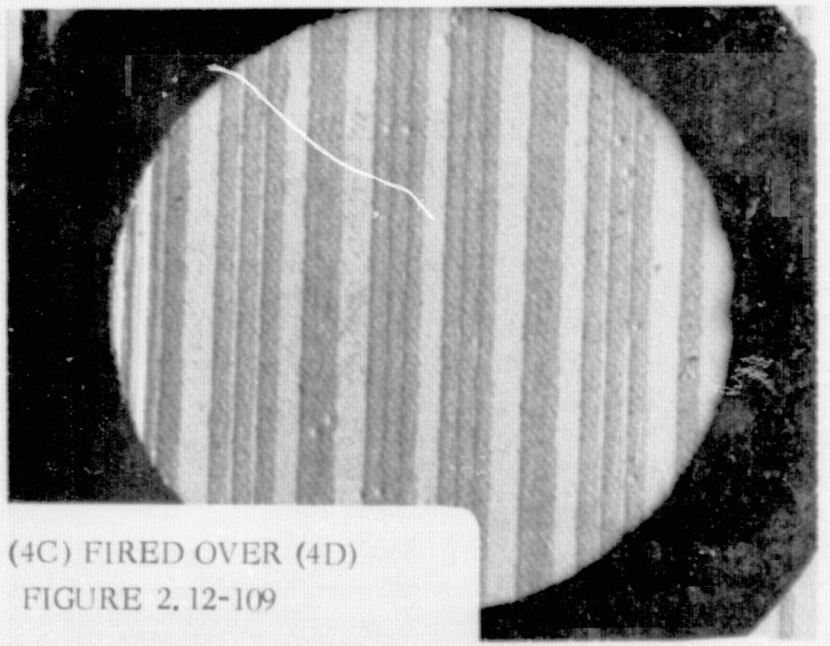
ENGELHARD GOLD (A2789
(4C) FIRED OVER (1D)
FIGURE 2.12-106



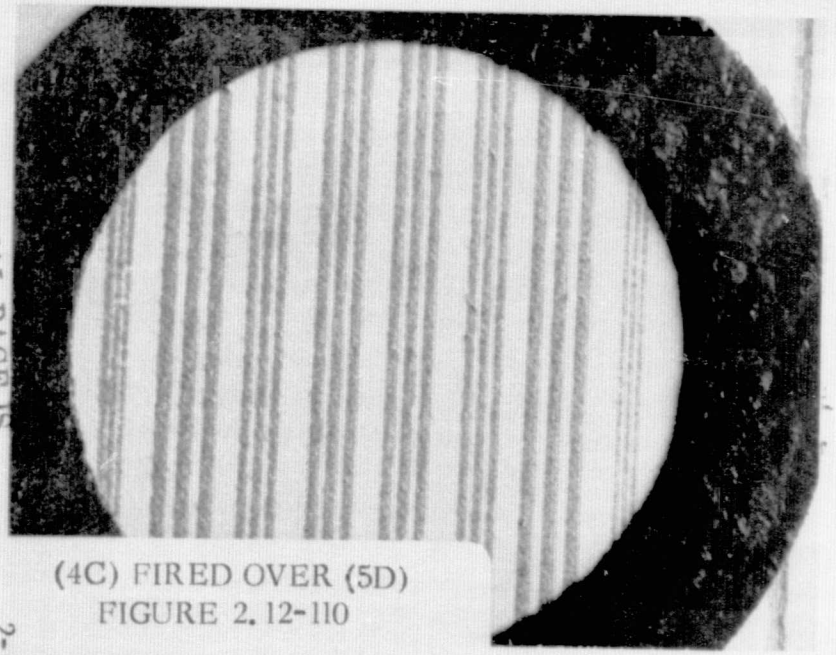
(4C) FIRED OVER (2D)
FIGURE 2.12-107



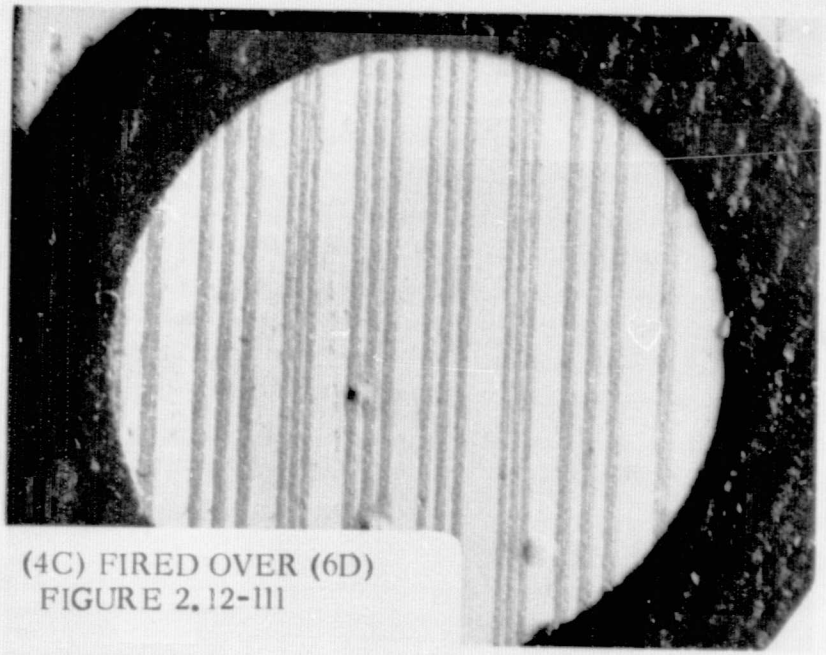
(4C) FIRED OVER (3D)
FIGURE 2.12-108



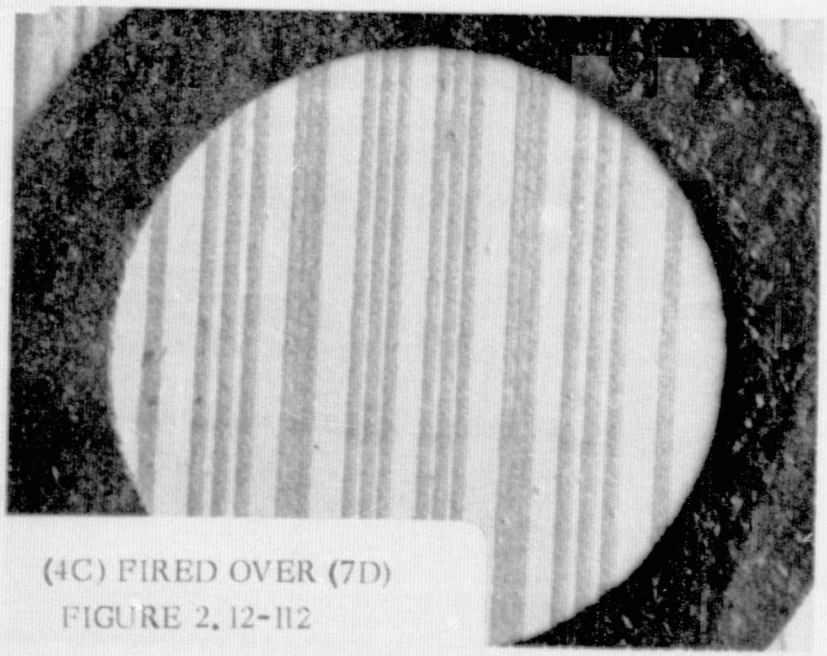
(4C) FIRED OVER (4D)
FIGURE 2.12-109



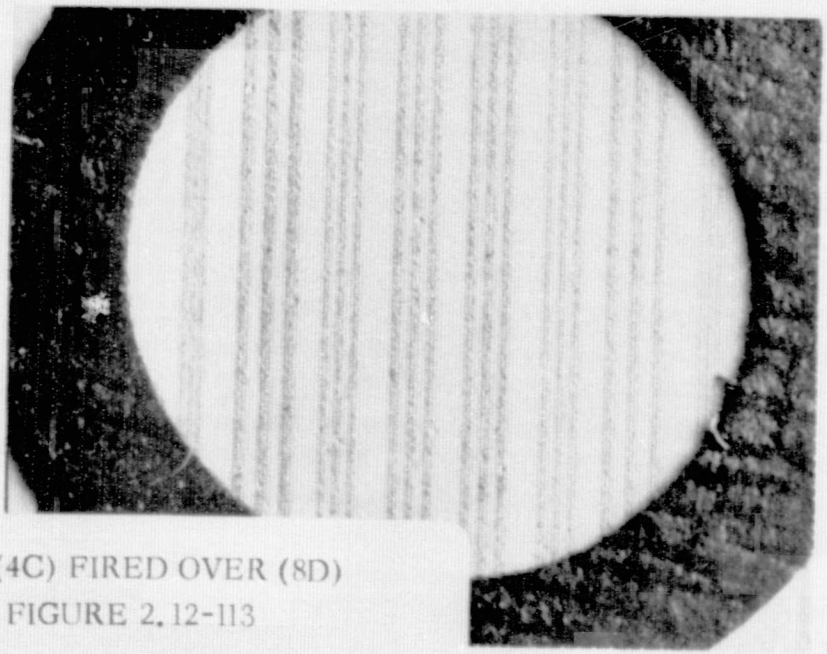
(4C) FIRED OVER (5D)
FIGURE 2.12-110



(4C) FIRED OVER (6D)
FIGURE 2.12-111

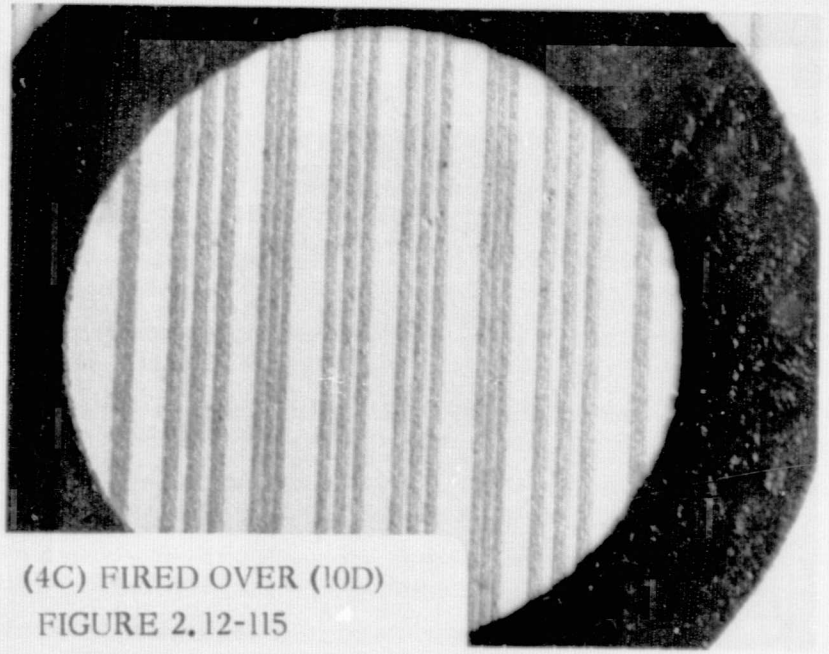


(4C) FIRED OVER (7D)
FIGURE 2.12-112

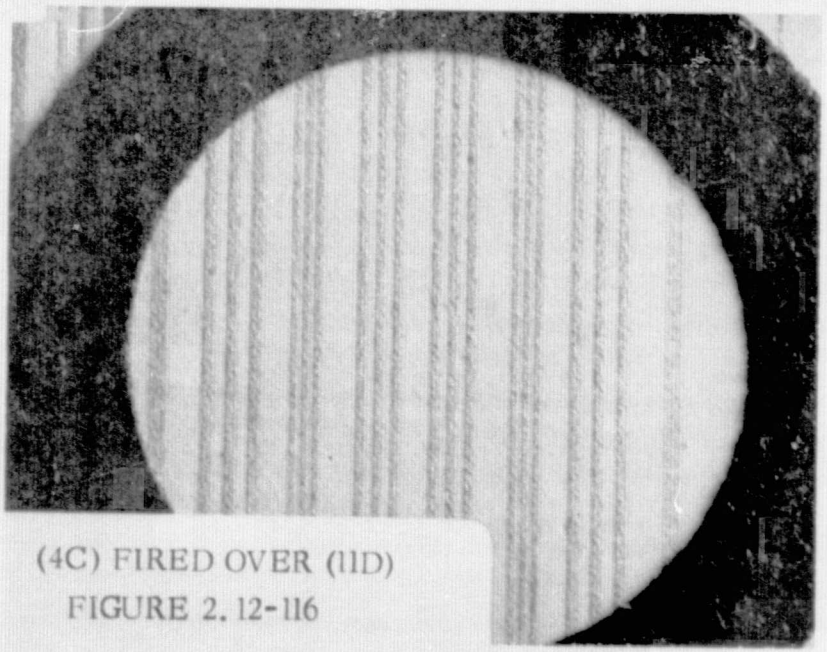


(4C) FIRED OVER (8D)
FIGURE 2.12-113

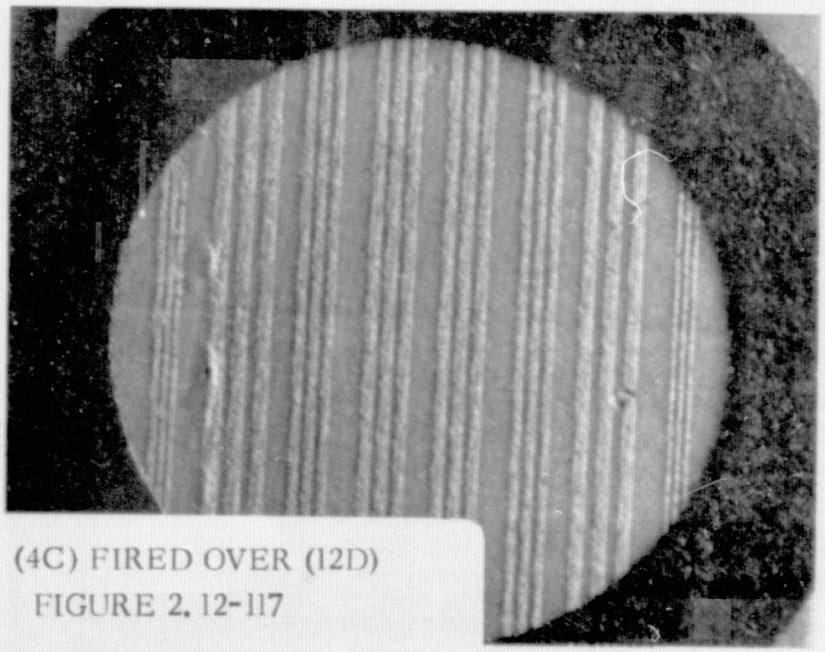
(4C) FIRED OVER (9D)
FIGURE 2.12-114



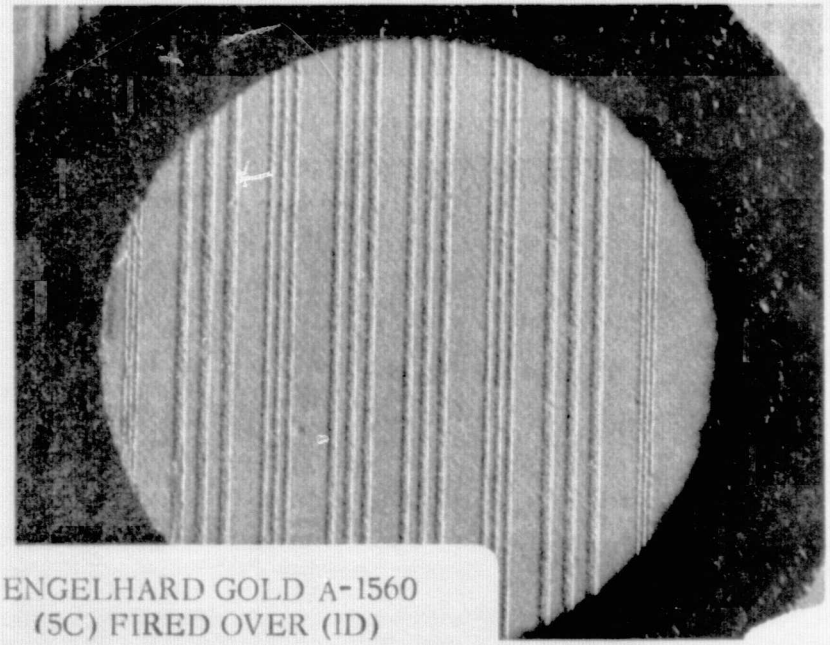
(4C) FIRED OVER (10D)
FIGURE 2.12-115



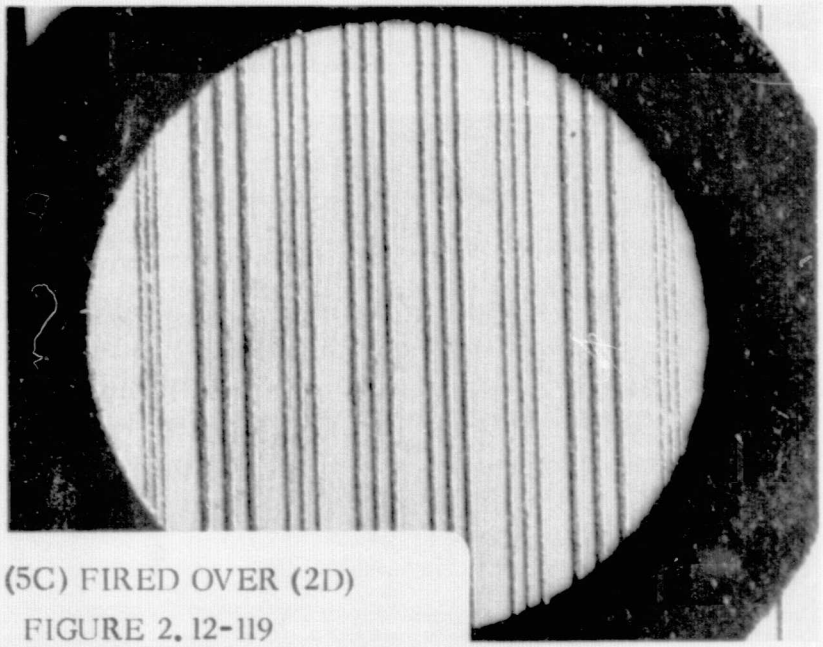
(4C) FIRED OVER (11D)
FIGURE 2.12-116



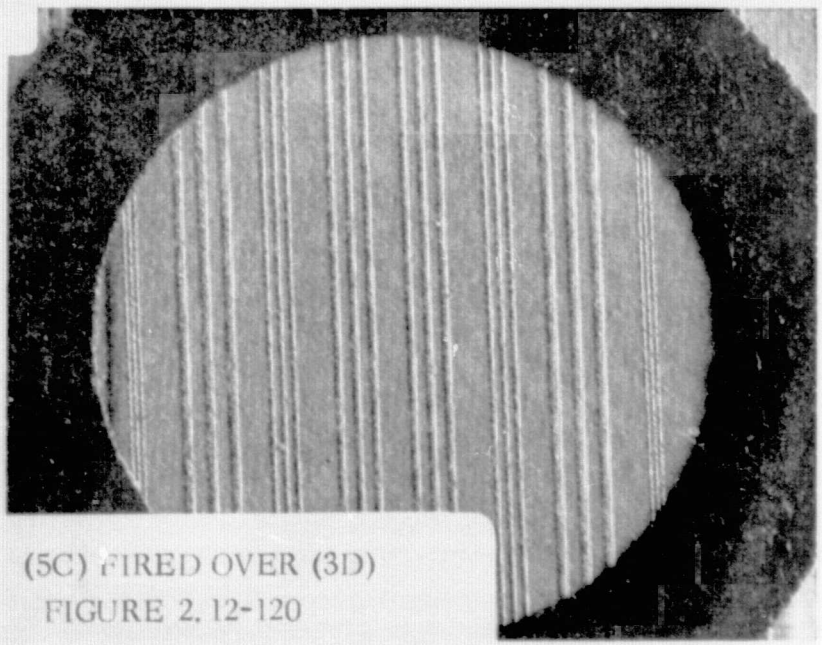
(4C) FIRED OVER (12D)
FIGURE 2.12-117



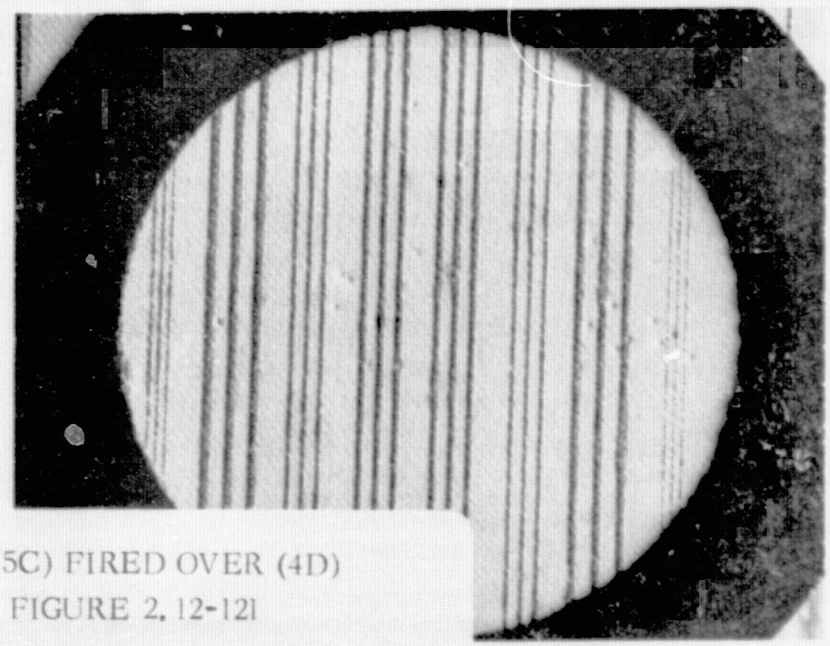
ENGELHARD GOLD A-1560
(5C) FIRED OVER (1D)
FIGURE 2.12-118



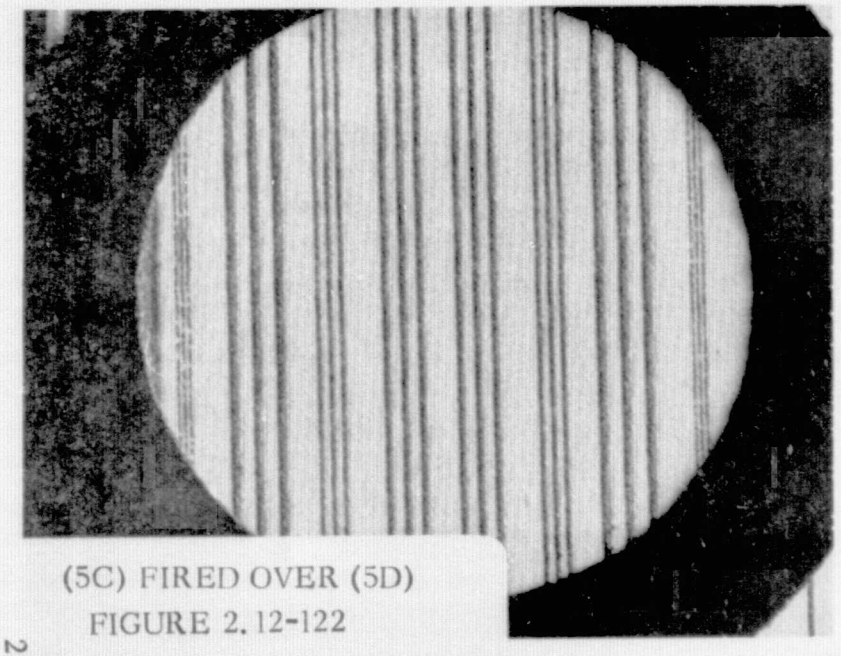
(5C) FIRED OVER (2D)
FIGURE 2.12-119



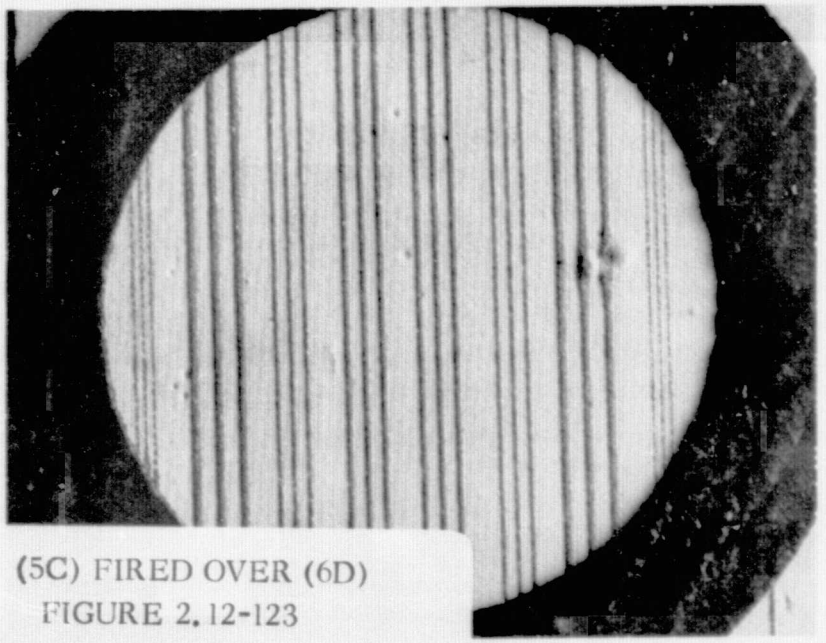
(5C) FIRED OVER (3D)
FIGURE 2.12-120



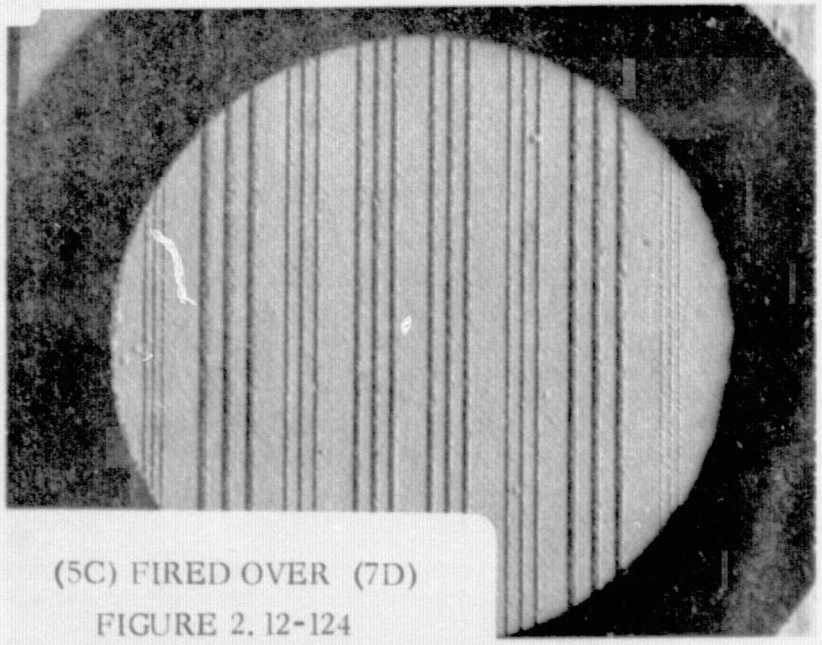
(5C) FIRED OVER (4D)
FIGURE 2.12-121



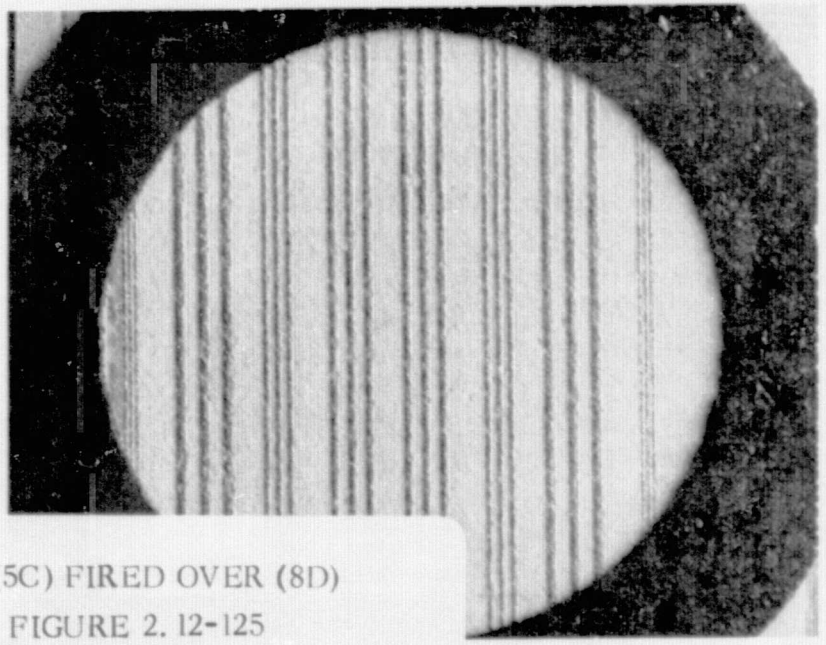
(5C) FIRED OVER (5D)
FIGURE 2.12-122



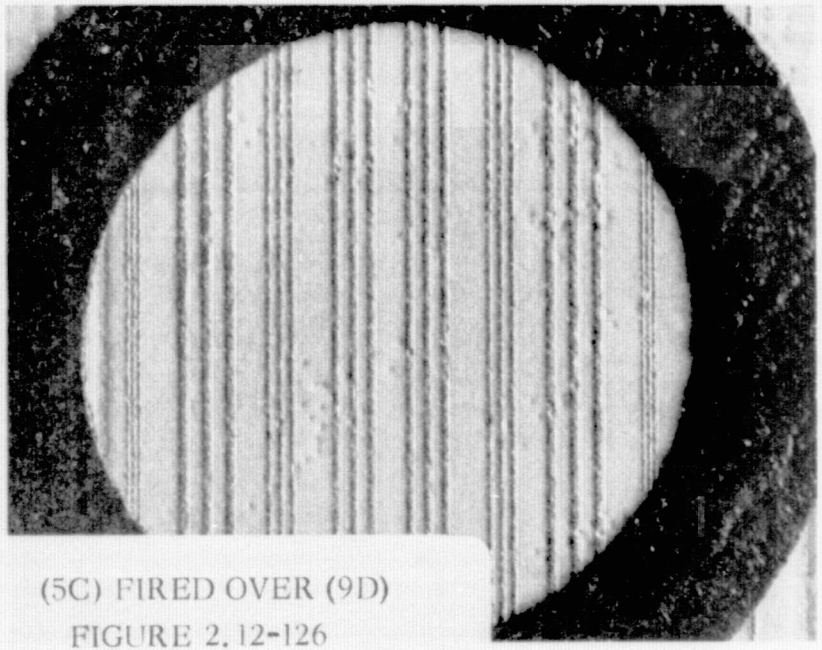
(5C) FIRED OVER (6D)
FIGURE 2.12-123



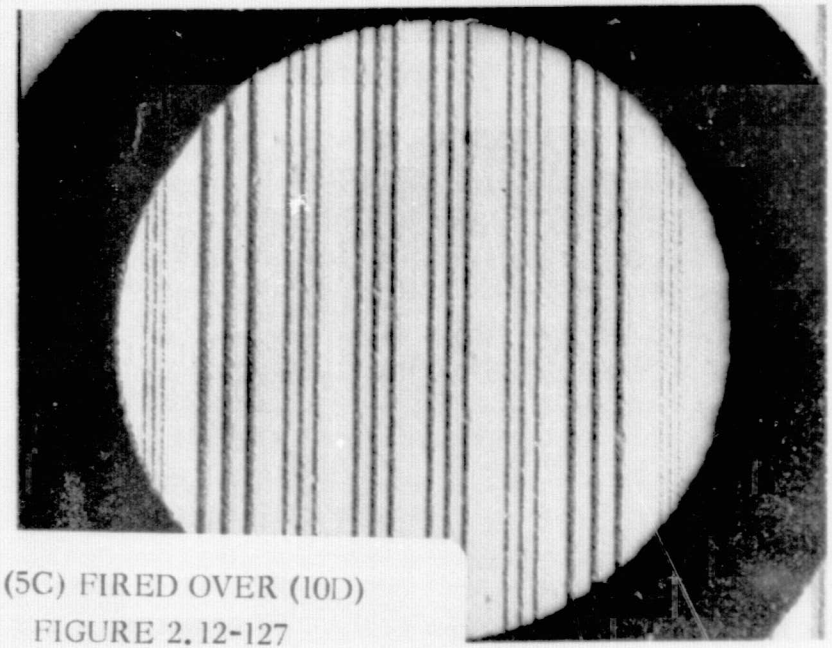
(5C) FIRED OVER (7D)
FIGURE 2.12-124



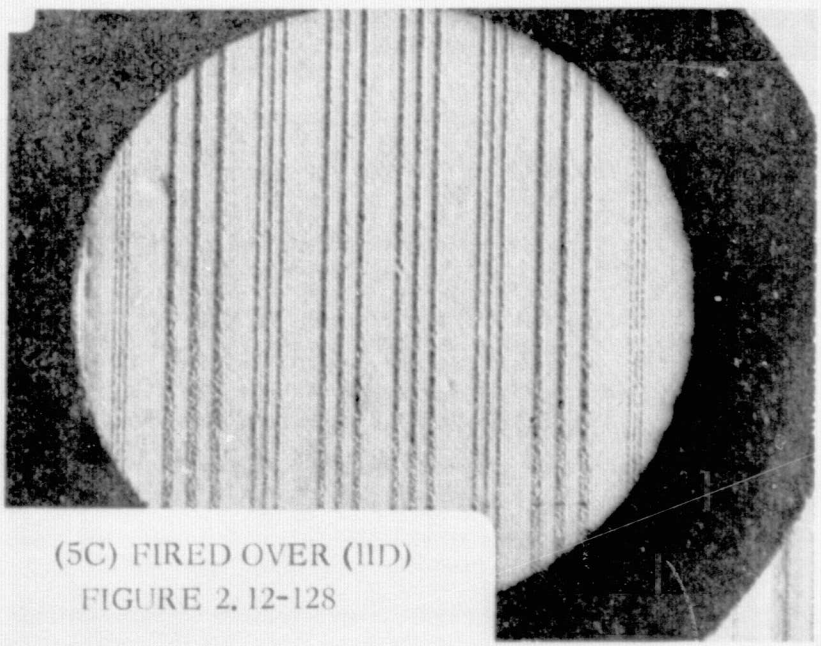
(5C) FIRED OVER (8D)
FIGURE 2.12-125



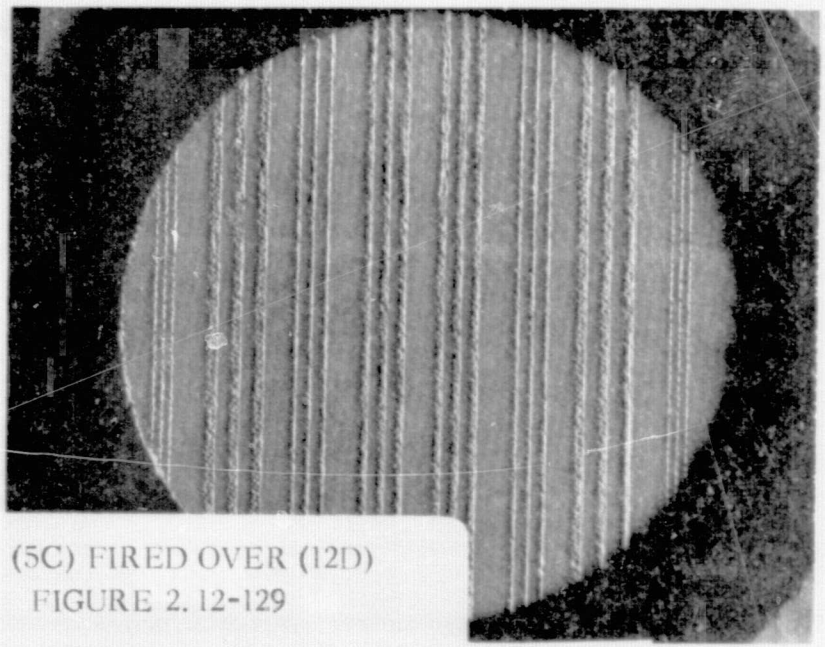
(5C) FIRED OVER (9D)
FIGURE 2.12-126



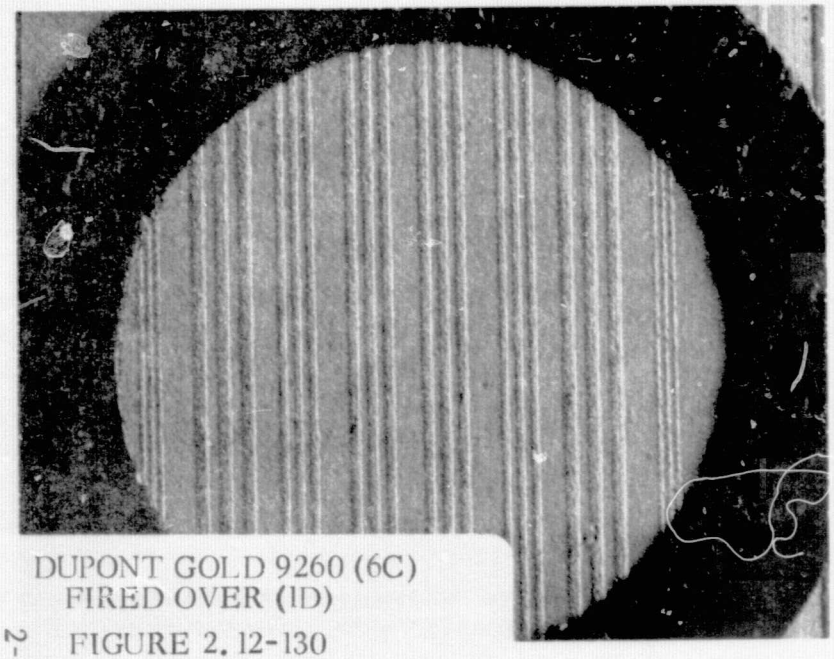
(5C) FIRED OVER (10D)
FIGURE 2.12-127



(5C) FIRED OVER (11D)
FIGURE 2.12-128

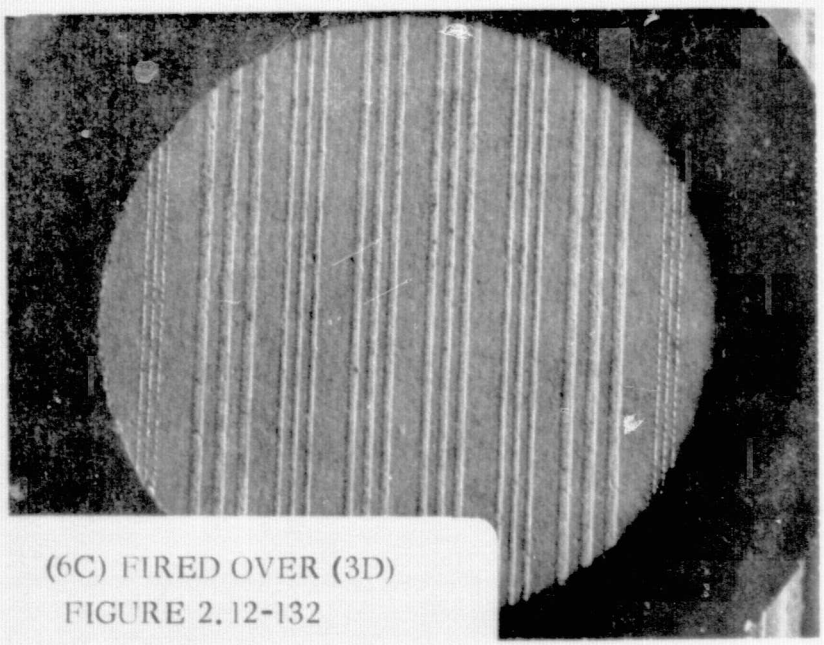


(5C) FIRED OVER (12D)
FIGURE 2.12-129

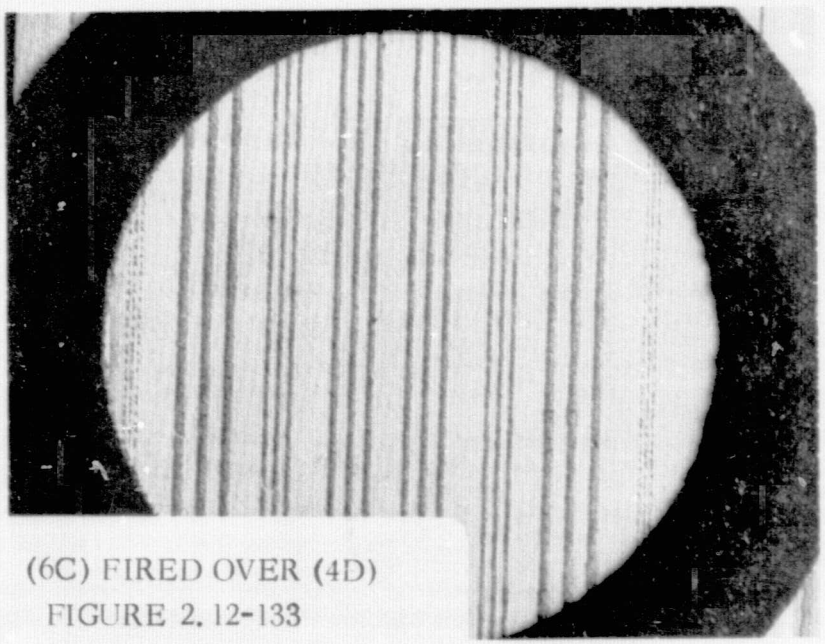


DUPONT GOLD 9260 (6C)
FIRED OVER (1D)
FIGURE 2.12-130

(6C) FIRED OVER (2D)
FIGURE 2.12-131



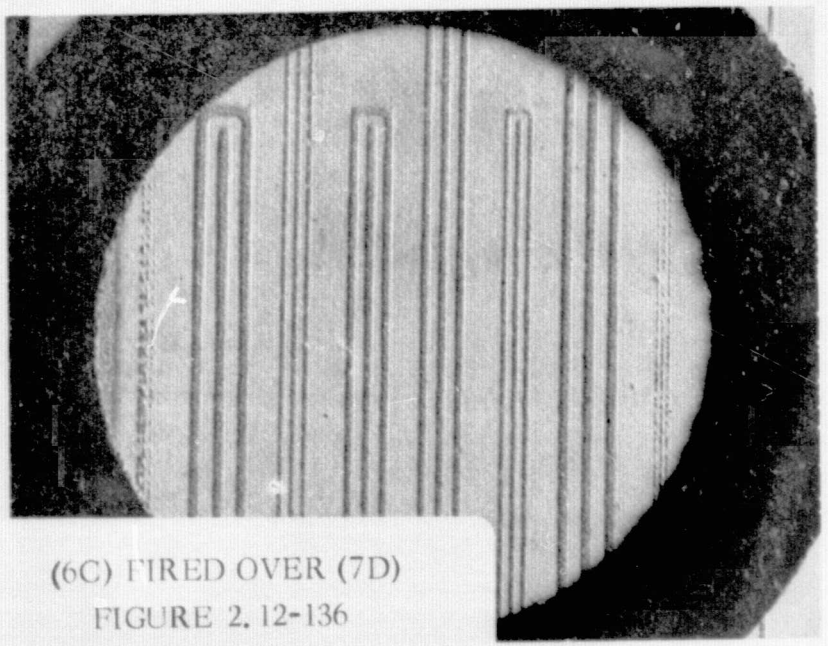
(6C) FIRED OVER (3D)
FIGURE 2.12-132



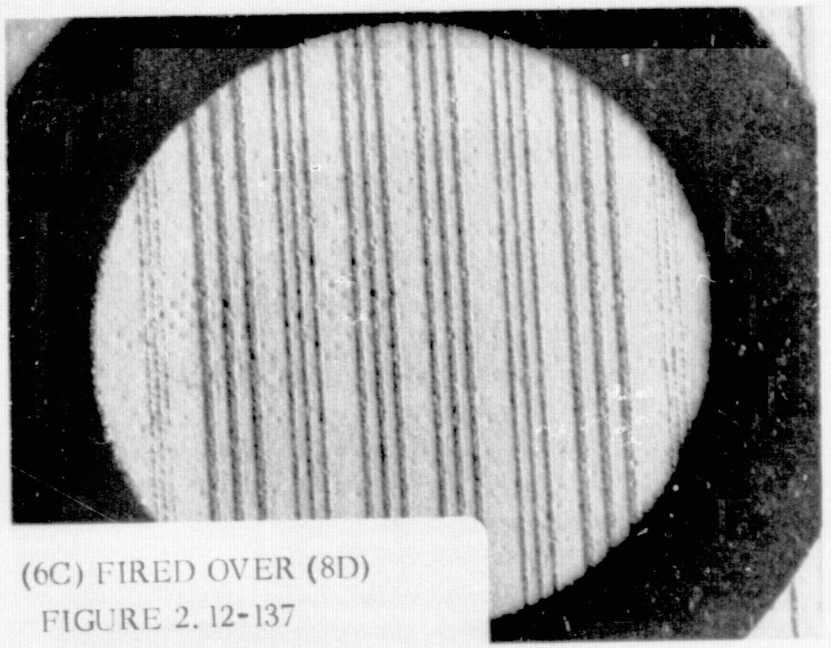
(6C) FIRED OVER (4D)
FIGURE 2.12-133

(6C) FIRED OVER (5D)
FIGURE 2. 12-134

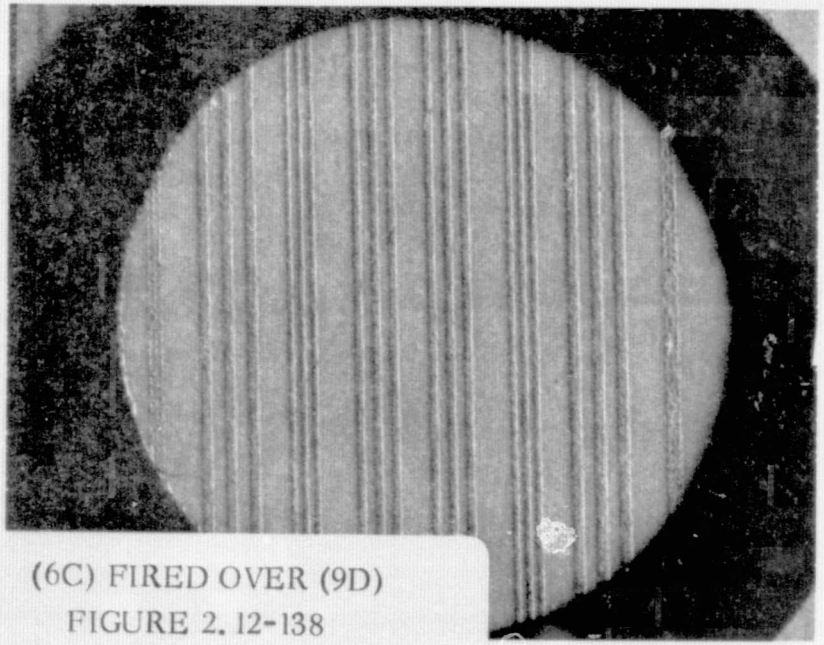
(6C) FIRED OVER (6D)
FIGURE 2. 12-135



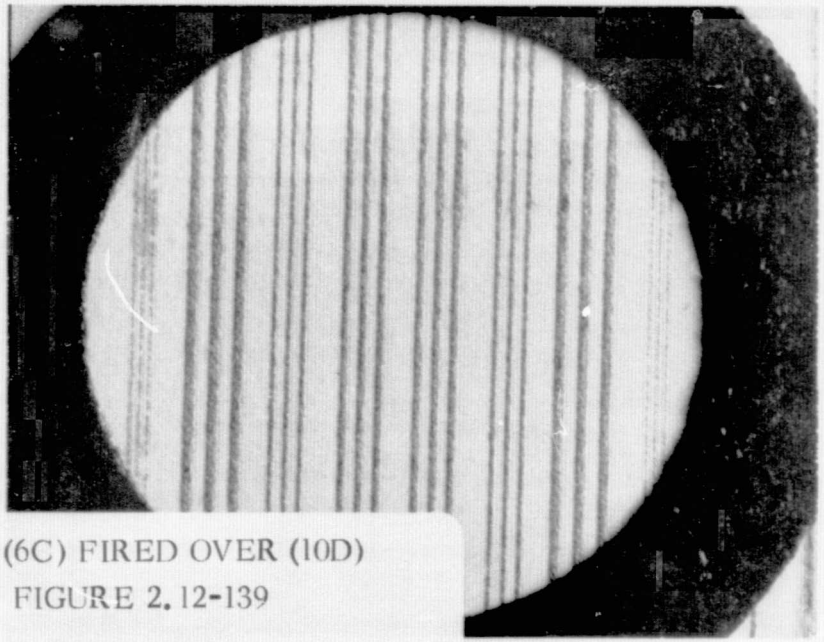
(6C) FIRED OVER (7D)
FIGURE 2. 12-136



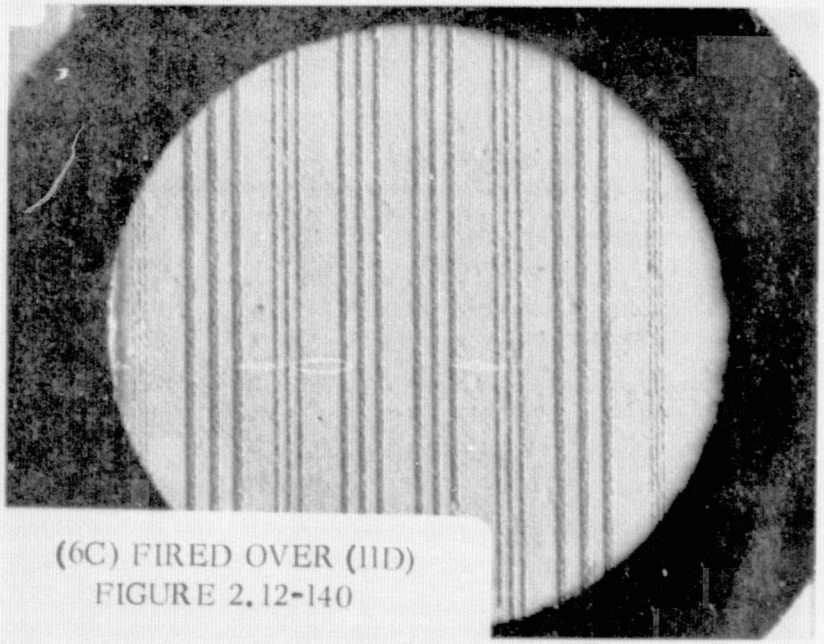
(6C) FIRED OVER (8D)
FIGURE 2. 12-137



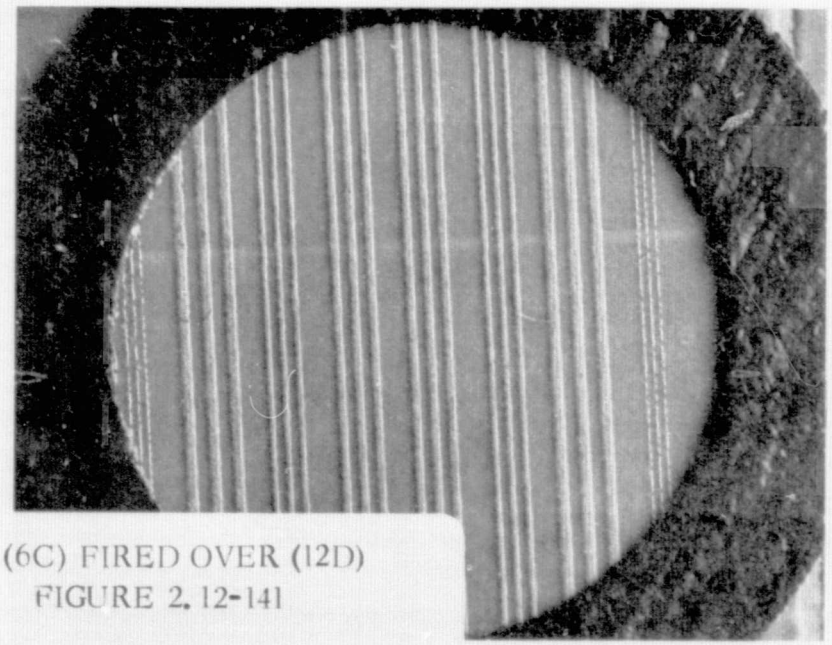
(6C) FIRED OVER (9D)
FIGURE 2.12-138



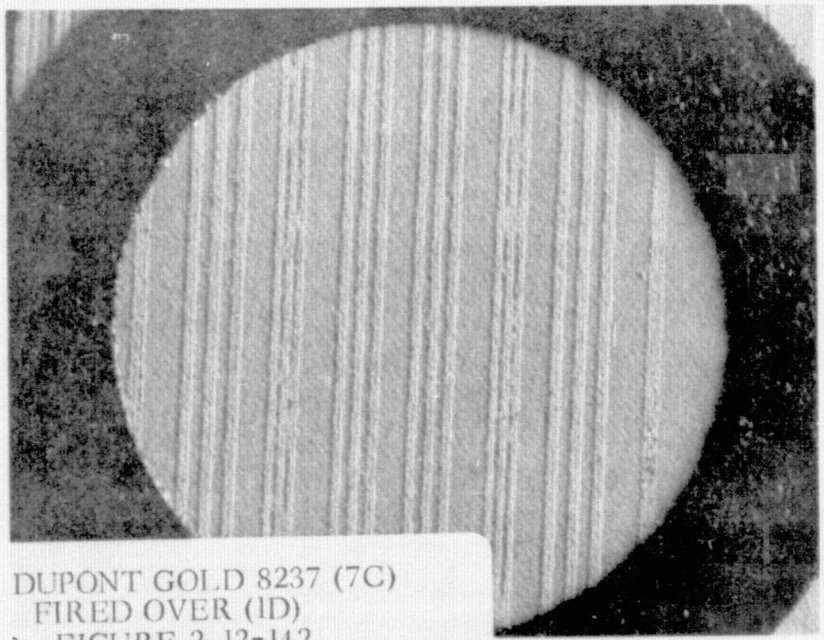
(6C) FIRED OVER (10D)
FIGURE 2.12-139



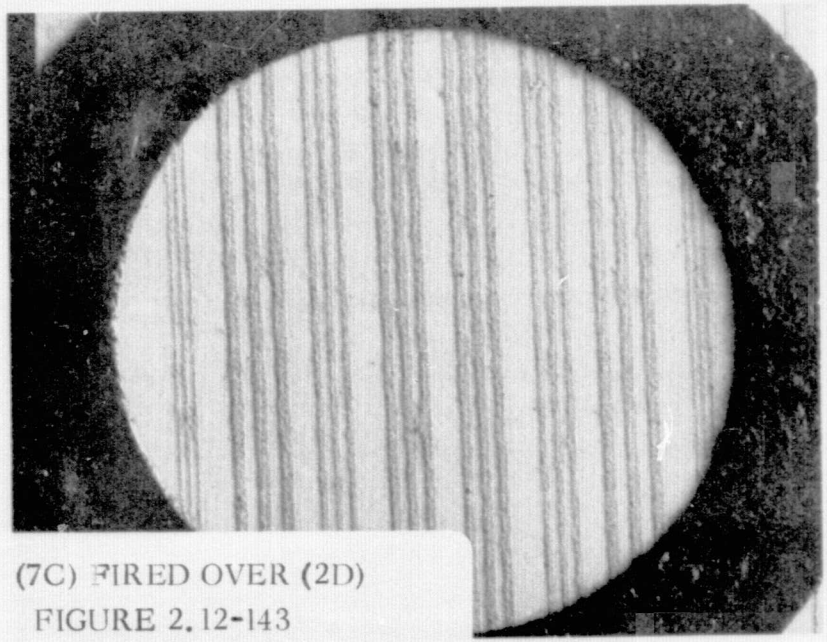
(6C) FIRED OVER (11D)
FIGURE 2.12-140



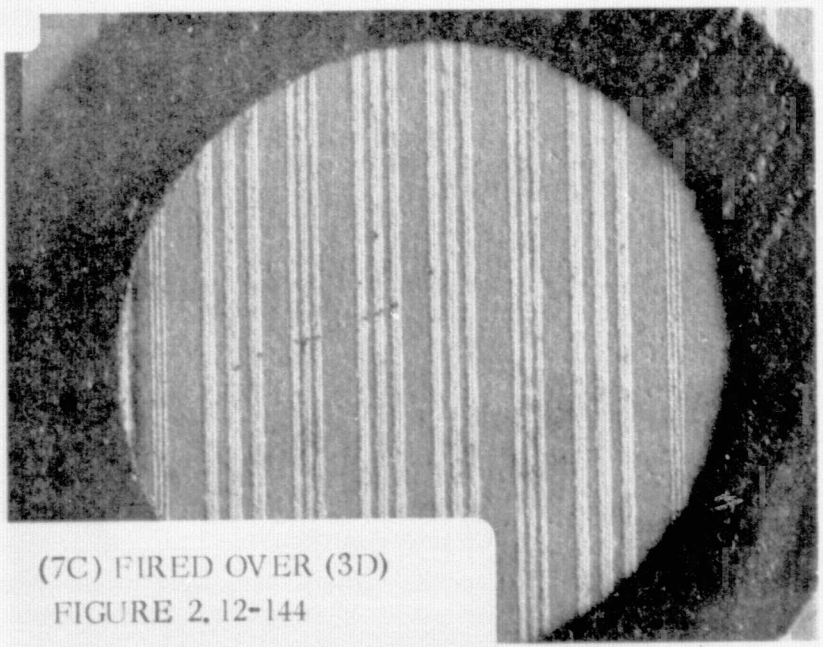
(6C) FIRED OVER (12D)
FIGURE 2.12-141



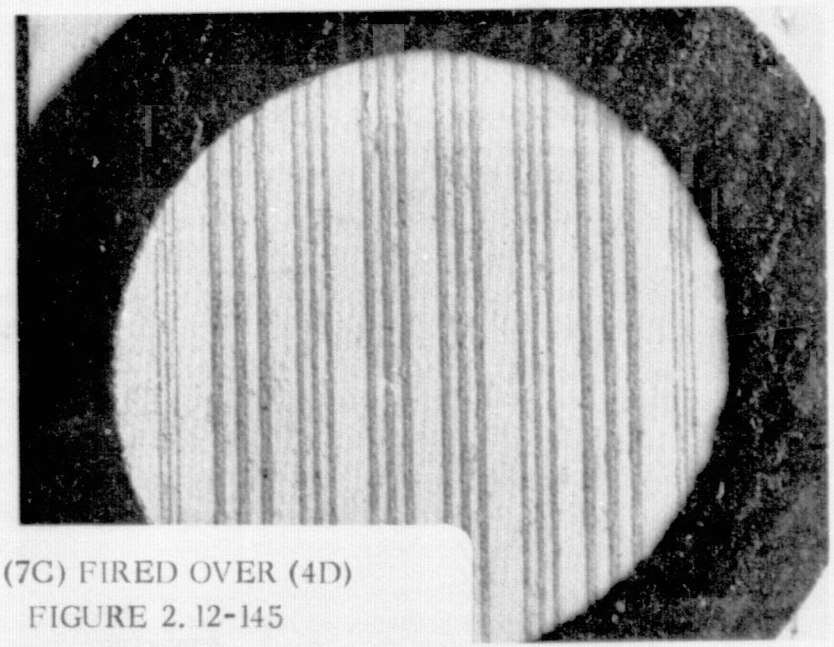
DUPONT GOLD 8237 (7C)
FIRED OVER (1D)
FIGURE 2.12-142



(7C) FIRED OVER (2D)
FIGURE 2.12-143

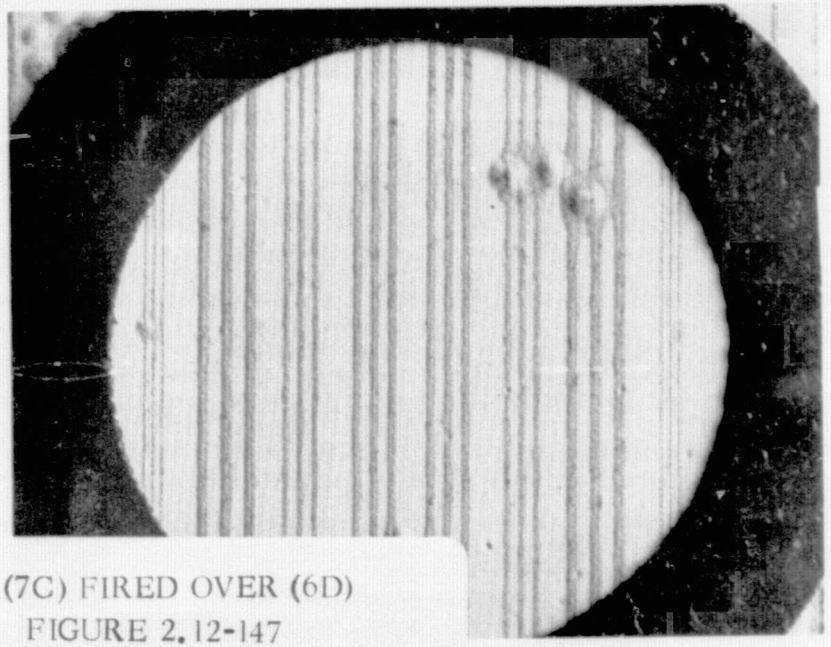


(7C) FIRED OVER (3D)
FIGURE 2.12-144

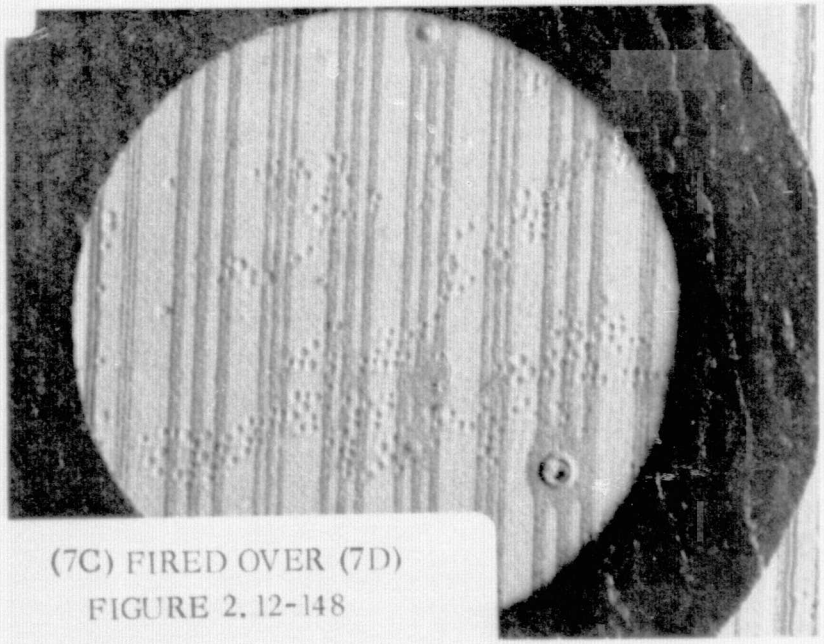


(7C) FIRED OVER (4D)
FIGURE 2.12-145

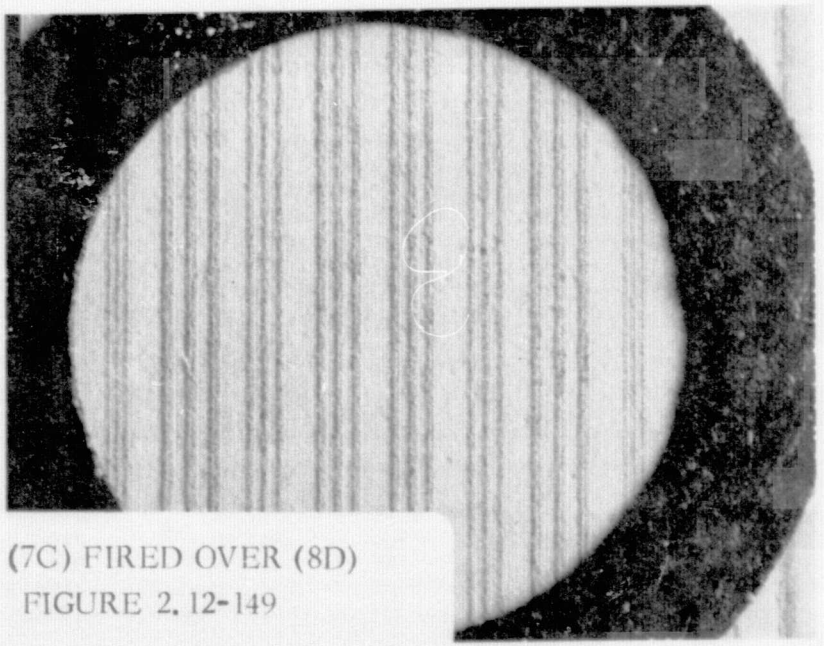
(7C) FIRED OVER (5D)
FIGURE 2.12-146



(7C) FIRED OVER (6D)
FIGURE 2.12-147



(7C) FIRED OVER (7D)
FIGURE 2.12-148



(7C) FIRED OVER (8D)
FIGURE 2.12-149

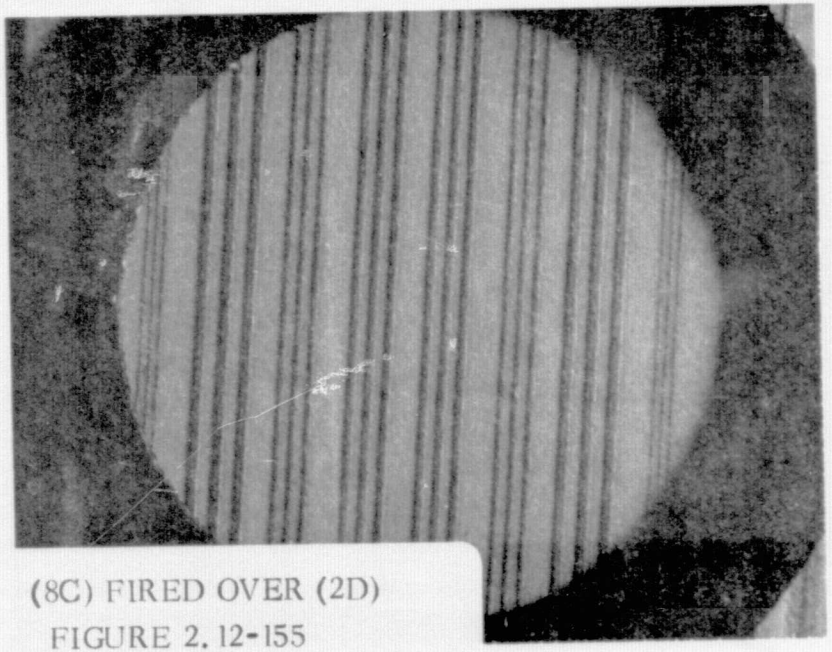
(7C) FIRED OVER (9D)
FIGURE 2. 12-150

(7C) FIRED OVER (10D)
FIGURE 2. 12-151

(7C) FIRED OVER (11D)
FIGURE 2. 12-152

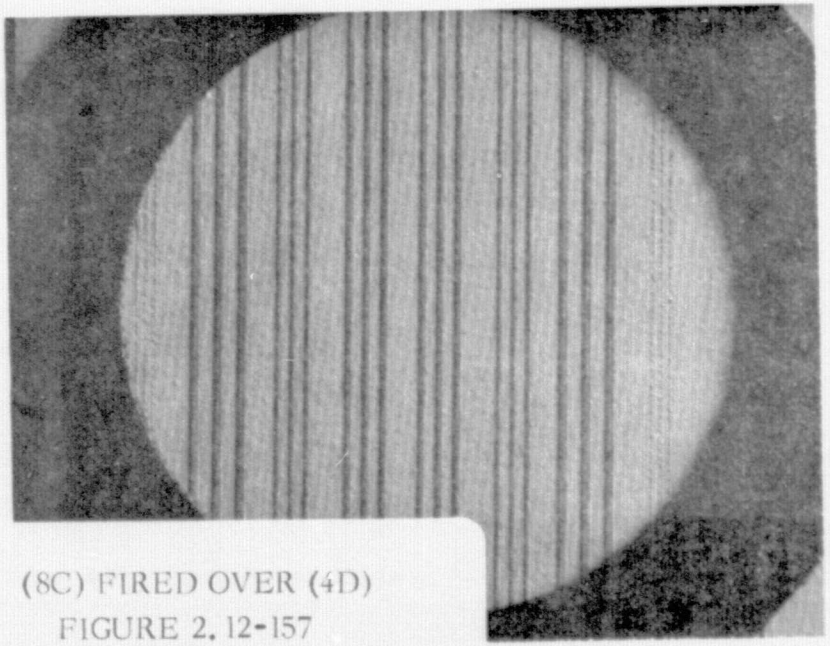
(7C) FIRED OVER (12D)
FIGURE 2. 12-153

ESL GOLD 8835-1B (8C)
FIRED OVER (1D)
FIGURE 2.12-154

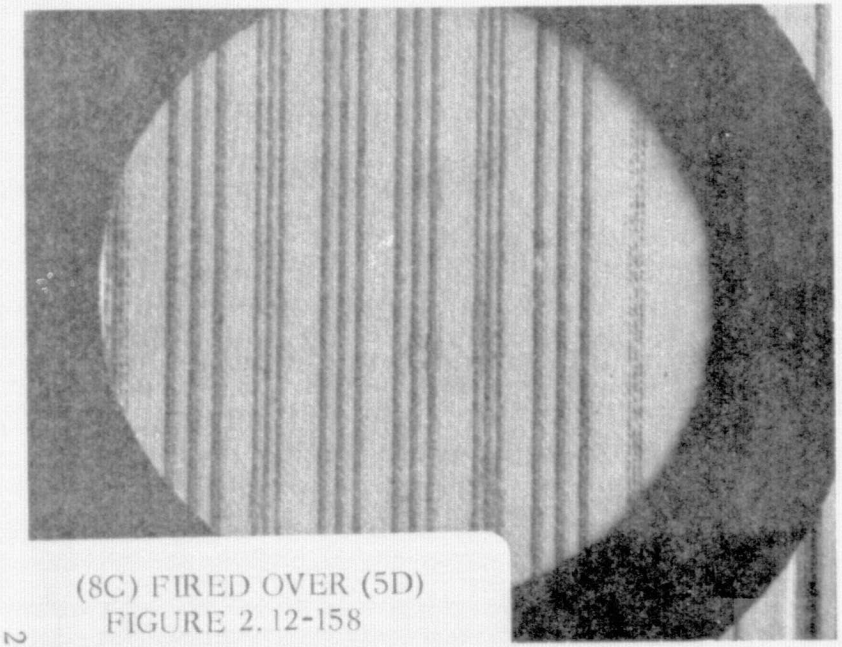


(8C) FIRED OVER (2D)
FIGURE 2.12-155

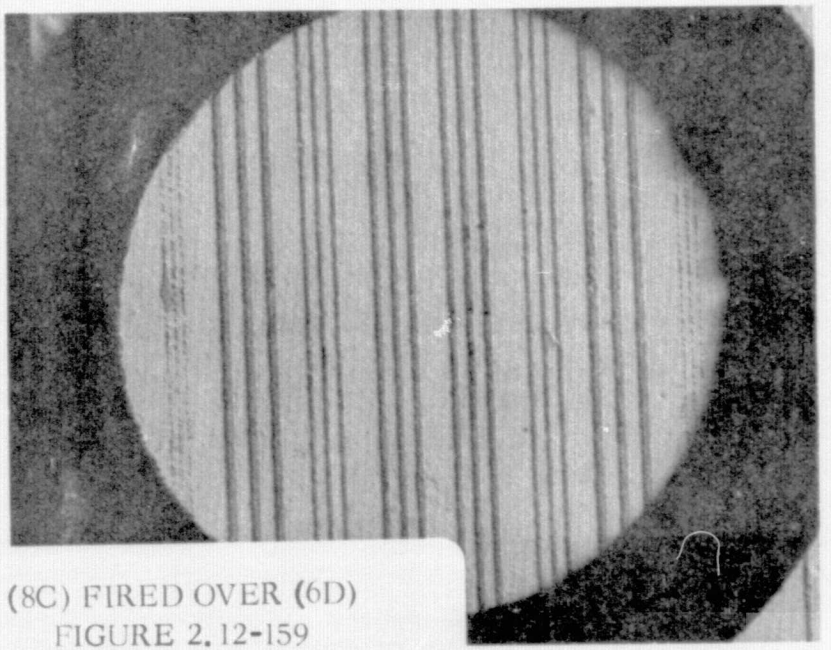
(8C) FIRED OVER (3D)
FIGURE 2.12-156



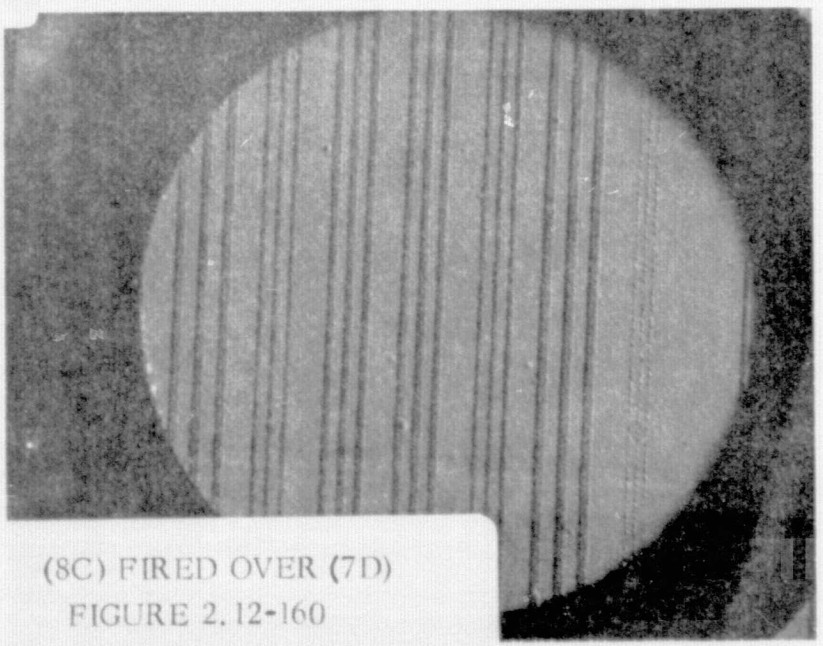
(8C) FIRED OVER (4D)
FIGURE 2.12-157



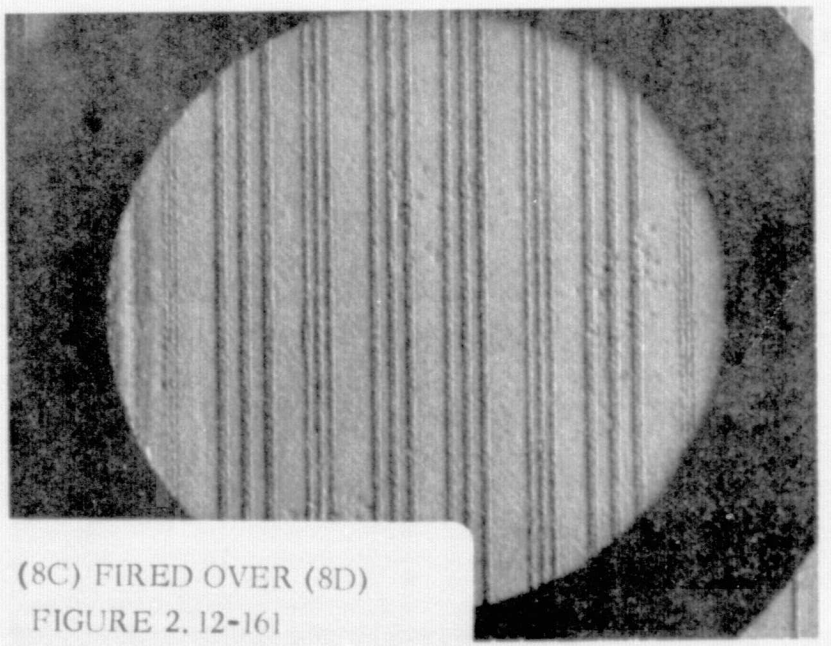
(8C) FIRED OVER (5D)
FIGURE 2.12-158



(8C) FIRED OVER (6D)
FIGURE 2.12-159

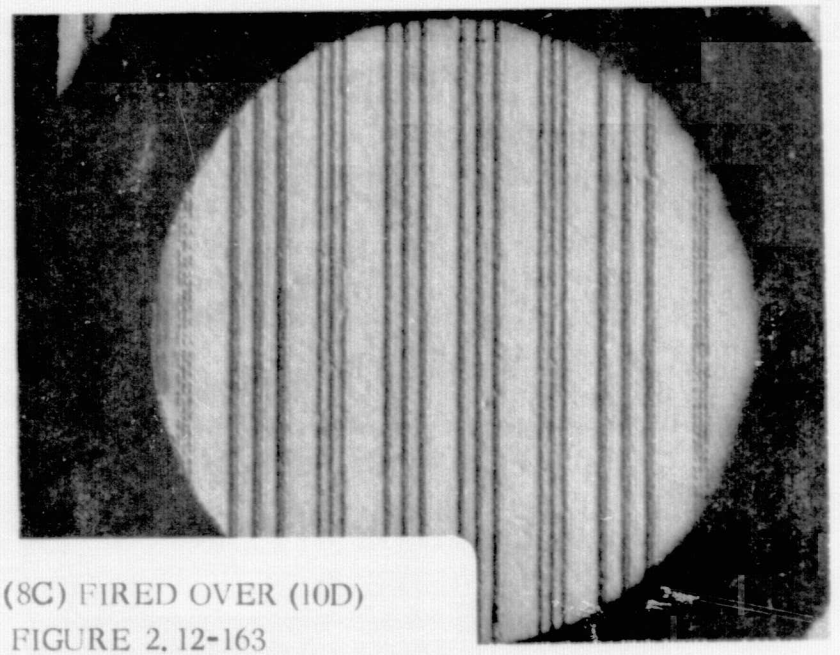


(8C) FIRED OVER (7D)
FIGURE 2.12-160

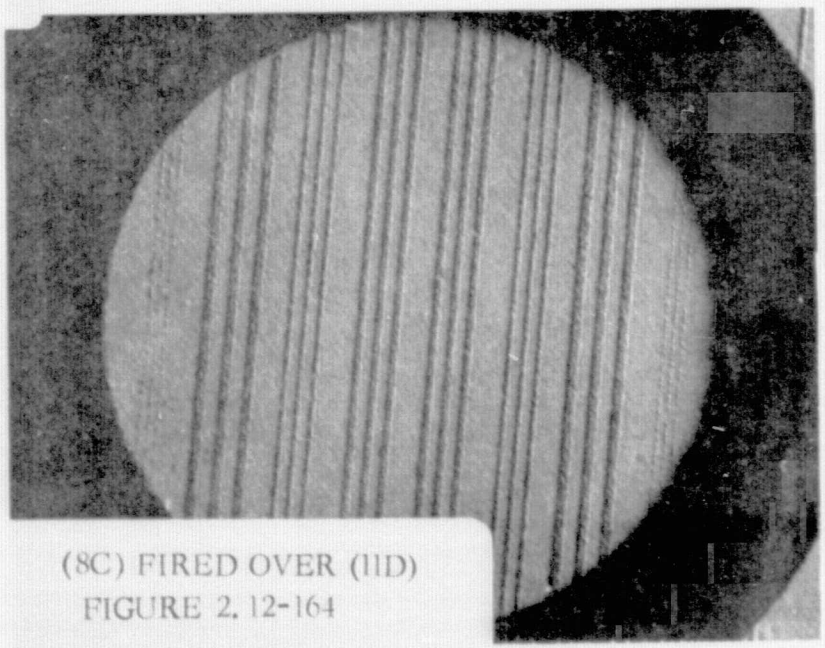


(8C) FIRED OVER (8D)
FIGURE 2.12-161

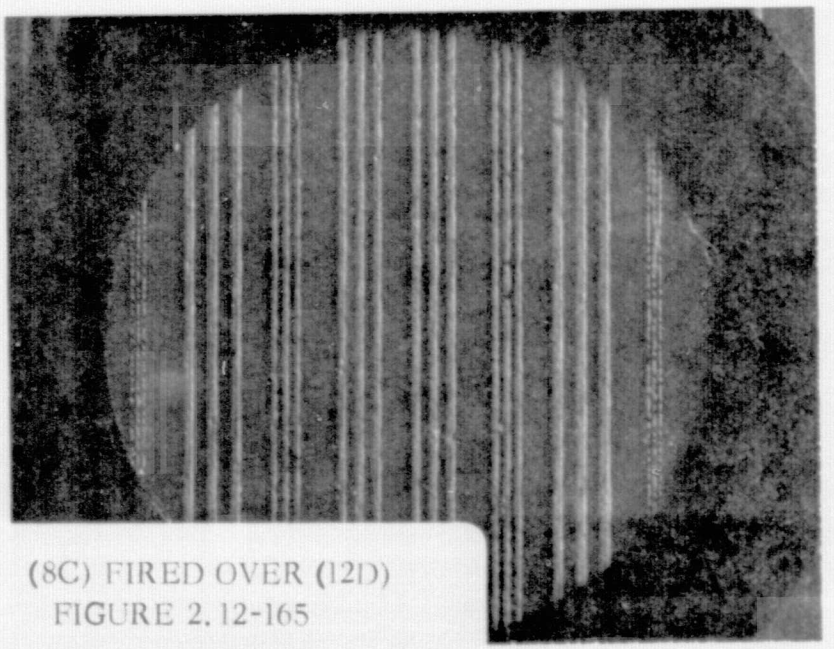
(8C) FIRED OVER (9D)
FIGURE 2.12-162



(8C) FIRED OVER (10D)
FIGURE 2.12-163



(8C) FIRED OVER (11D)
FIGURE 2.12-164



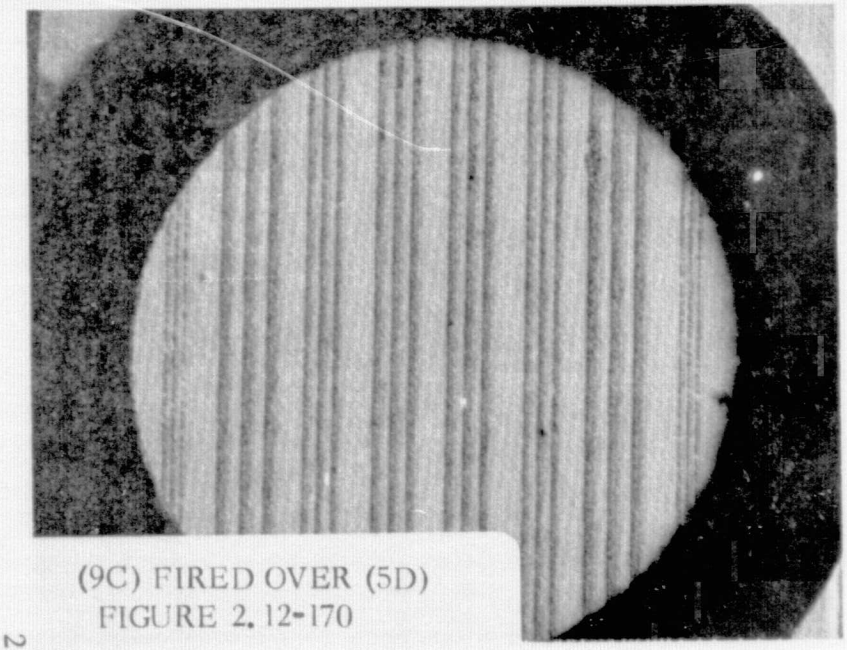
(8C) FIRED OVER (12D)
FIGURE 2.12-165

ESL GOLD 8835 (9C)
FIRED OVER (1D)
FIGURE 2.12-166

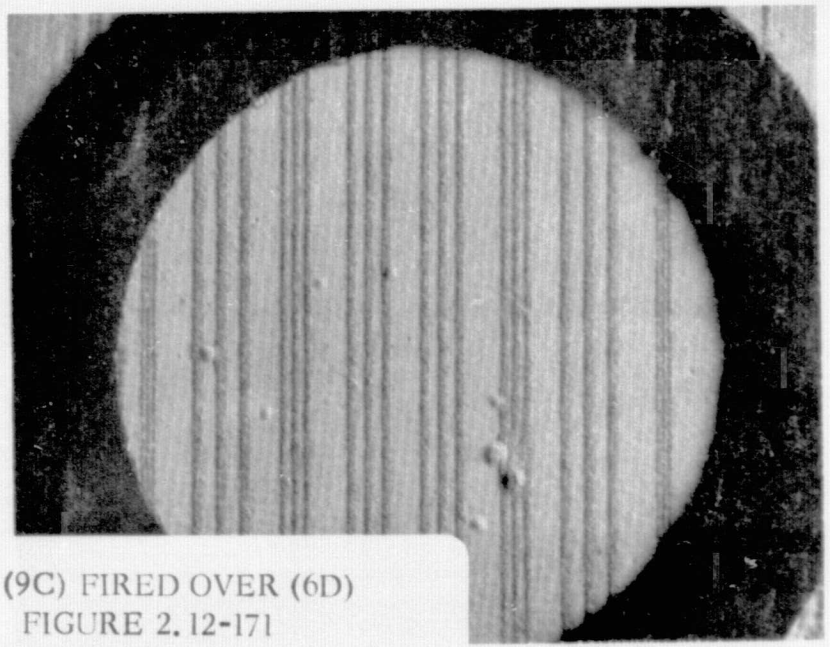
(9C) FIRED OVER (2D)
FIGURE 2.12-167

(9C) FIRED OVER (3D)
FIGURE 2.12-168

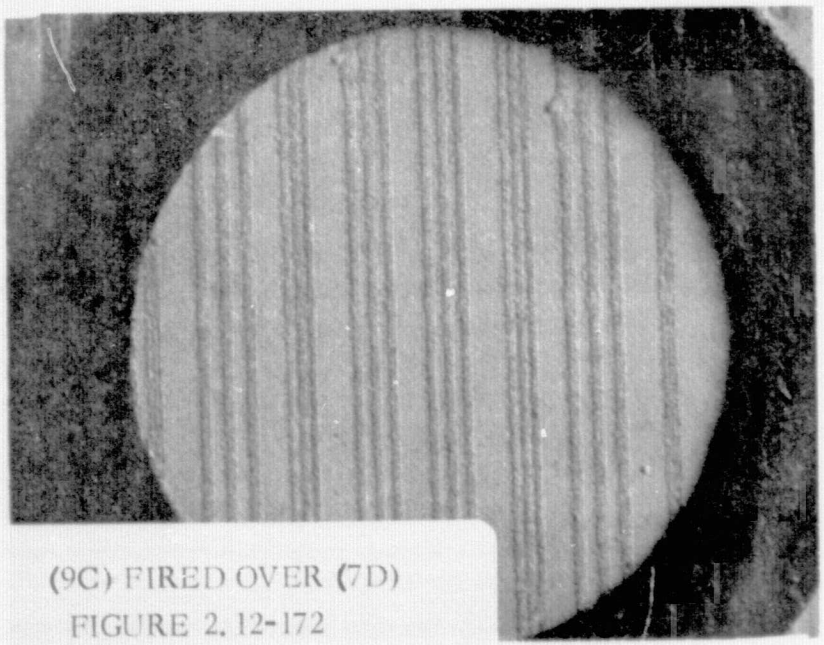
(9C) FIRED OVER (4D)
FIGURE 2.12-169



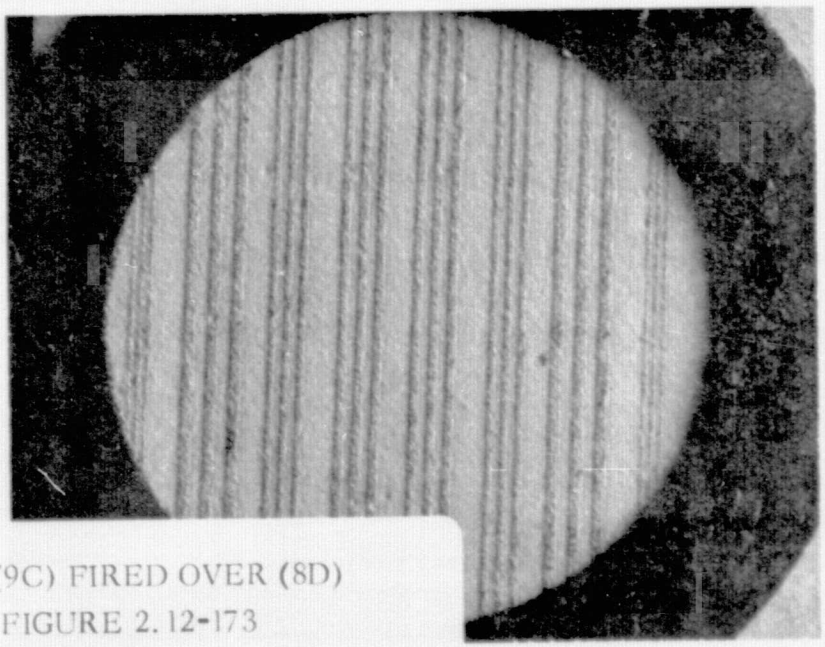
(9C) FIRED OVER (5D)
FIGURE 2.12-170



(9C) FIRED OVER (6D)
FIGURE 2.12-171



(9C) FIRED OVER (7D)
FIGURE 2.12-172



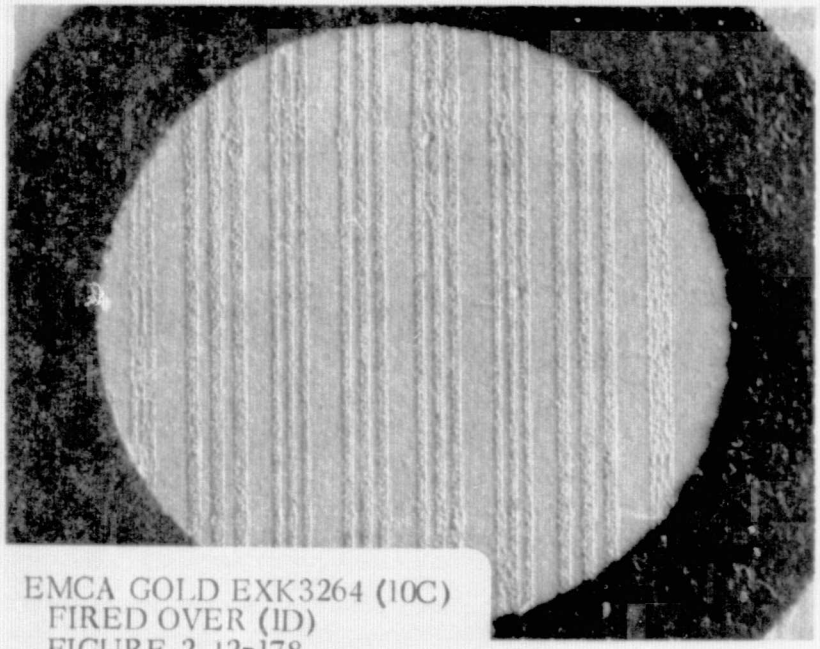
(9C) FIRED OVER (8D)
FIGURE 2.12-173

(9C) FIRED OVER (9D)
FIGURE 2.12-174

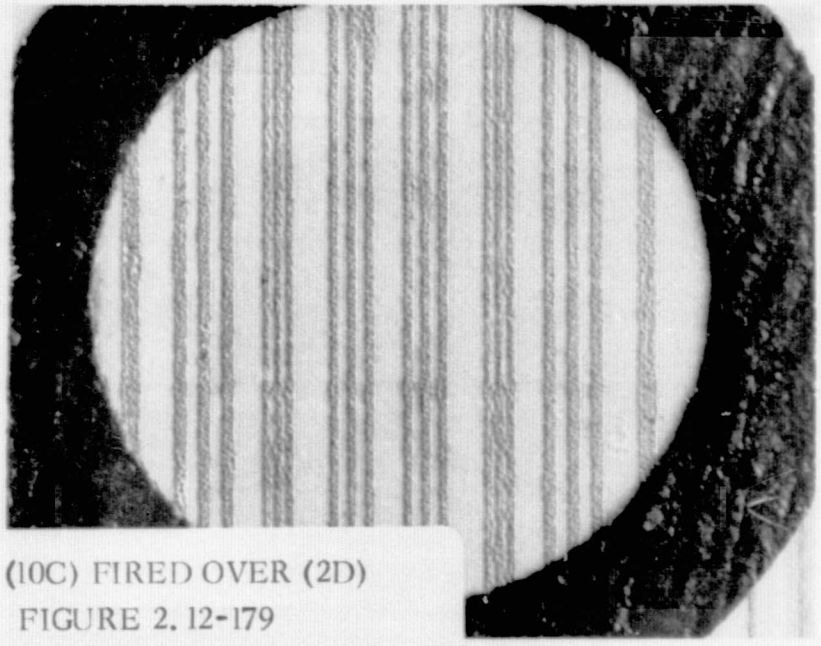
(9C) FIRED OVER (10D)
FIGURE 2.12-175

(9C) FIRED OVER (11D)
FIGURE 2.12-176

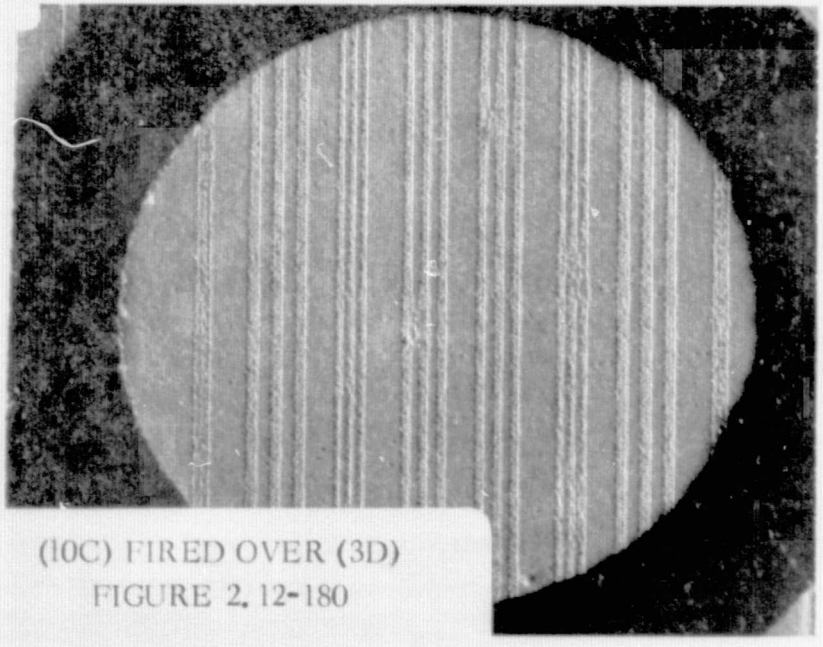
(9C) FIRED OVER (12D)
FIGURE 2.12-177



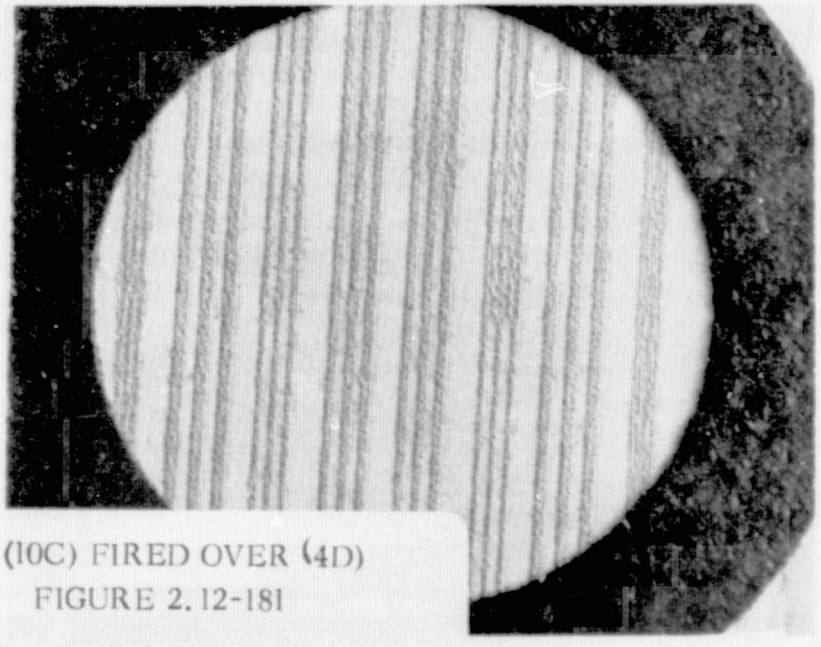
EMCA GOLD EXK3264 (10C)
FIRED OVER (1D)
FIGURE 2.12-178



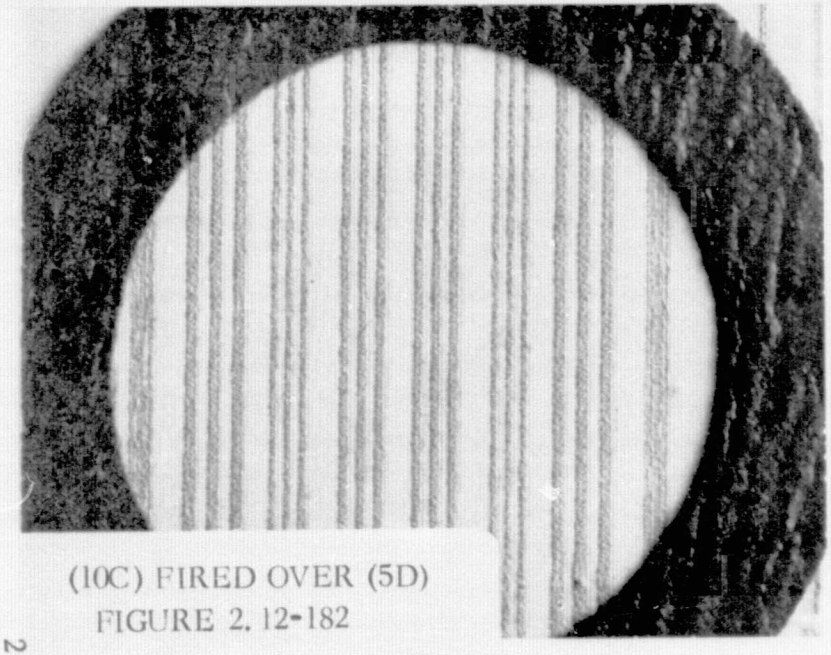
(10C) FIRED OVER (2D)
FIGURE 2.12-179



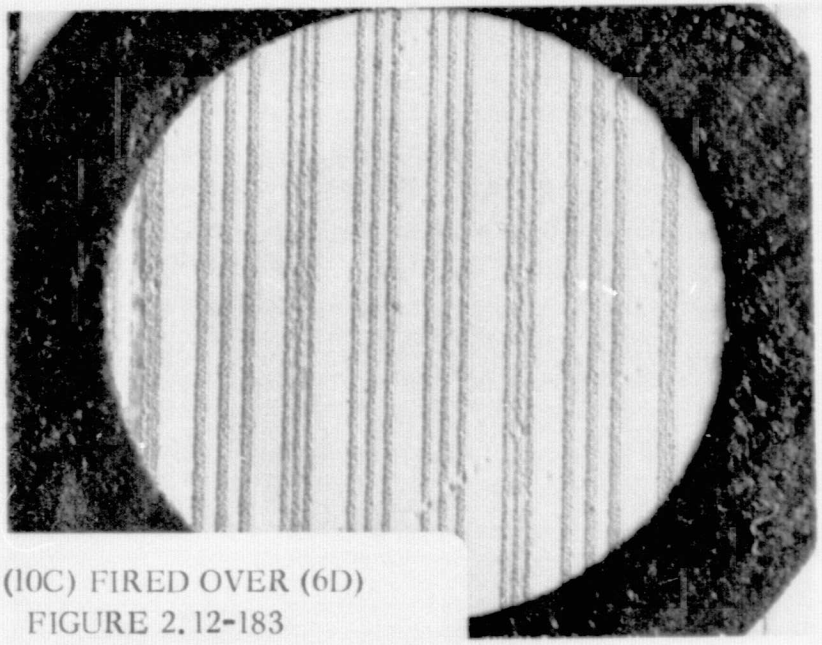
(10C) FIRED OVER (3D)
FIGURE 2.12-180



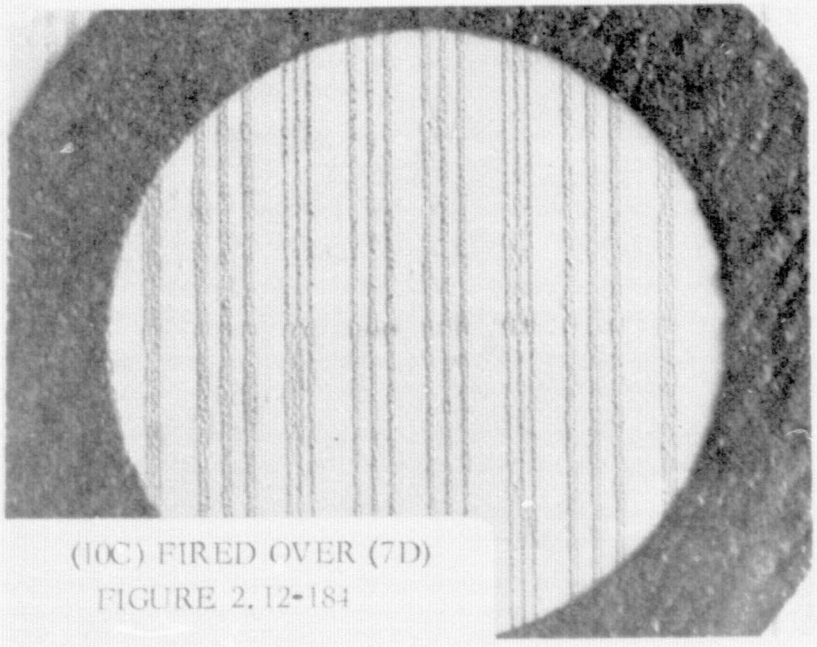
(10C) FIRED OVER (4D)
FIGURE 2.12-181



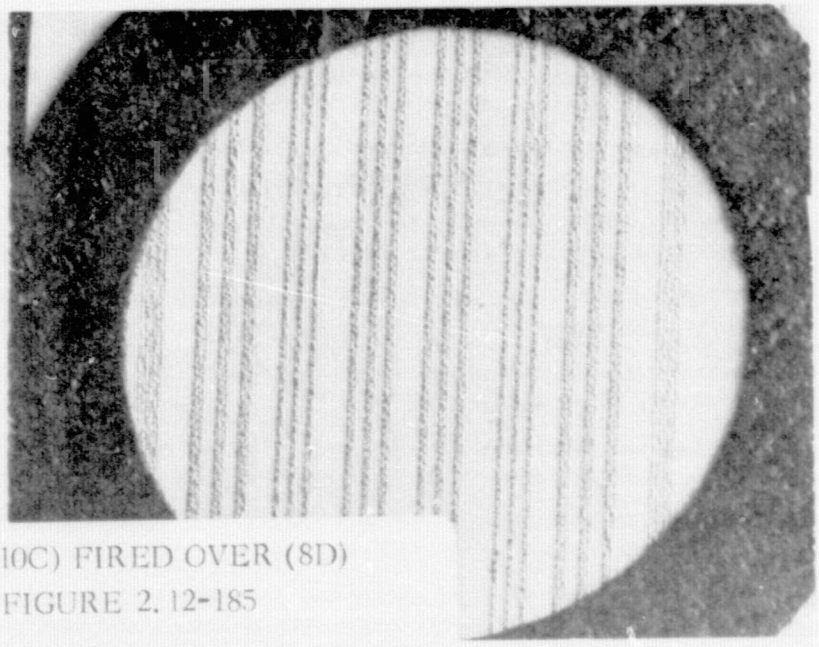
(10C) FIRED OVER (5D)
FIGURE 2.12-182



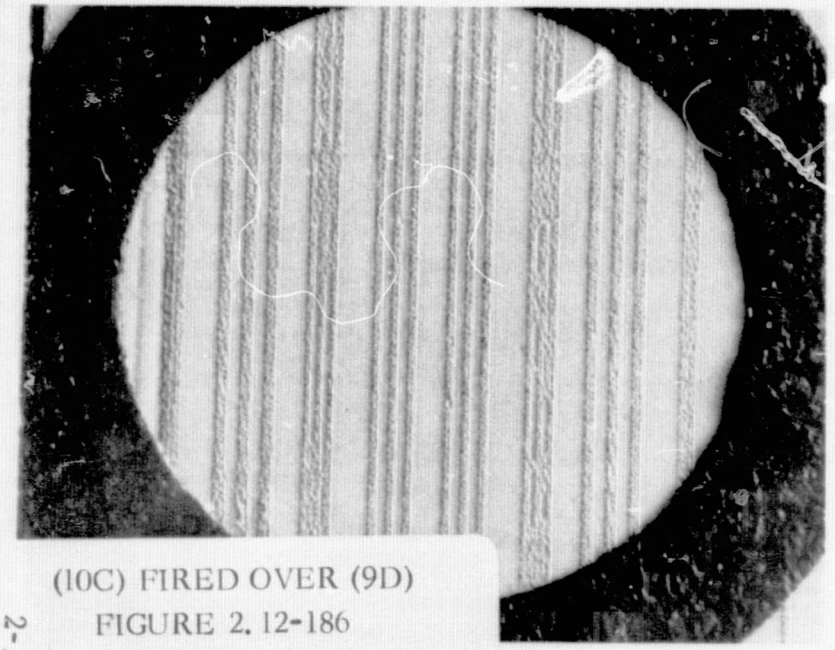
(10C) FIRED OVER (6D)
FIGURE 2.12-183



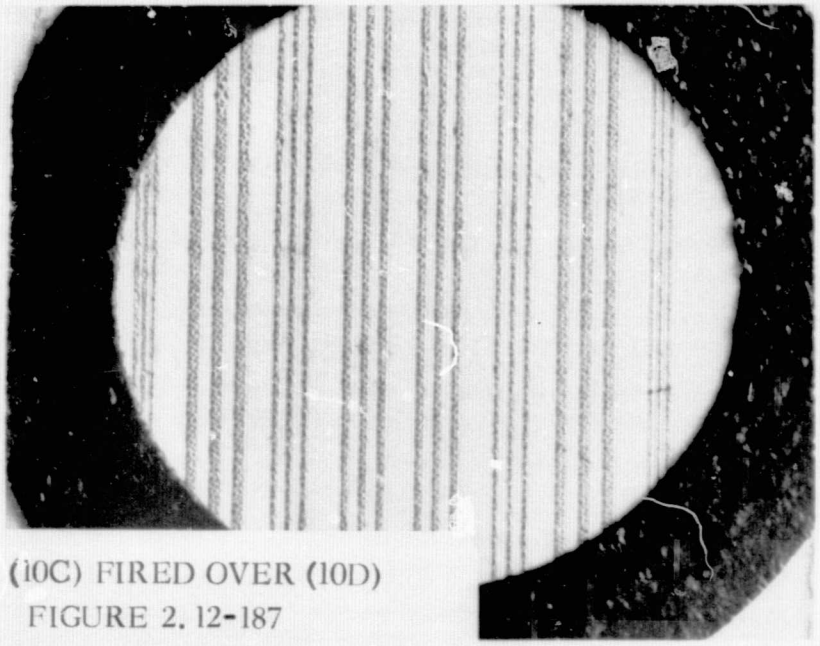
(10C) FIRED OVER (7D)
FIGURE 2.12-184



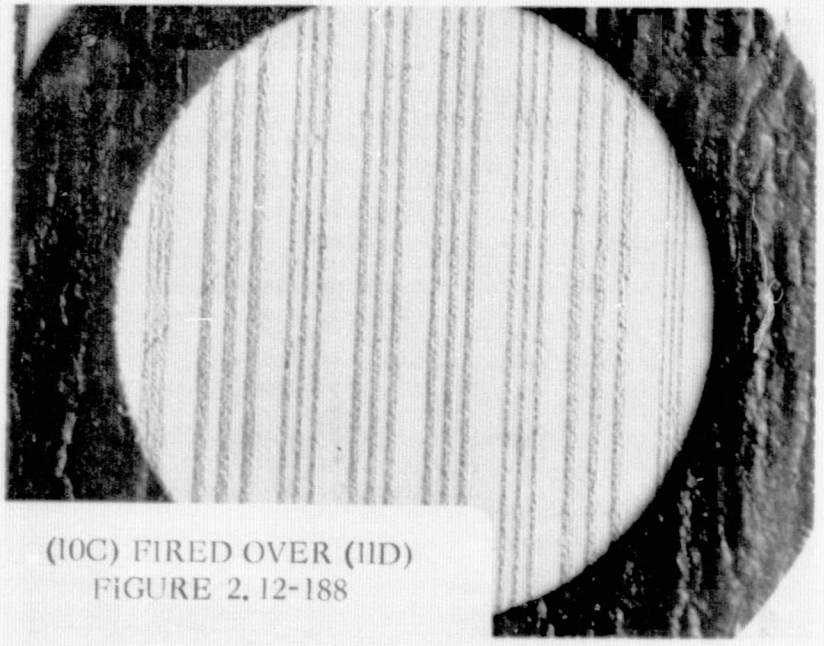
(10C) FIRED OVER (8D)
FIGURE 2.12-185



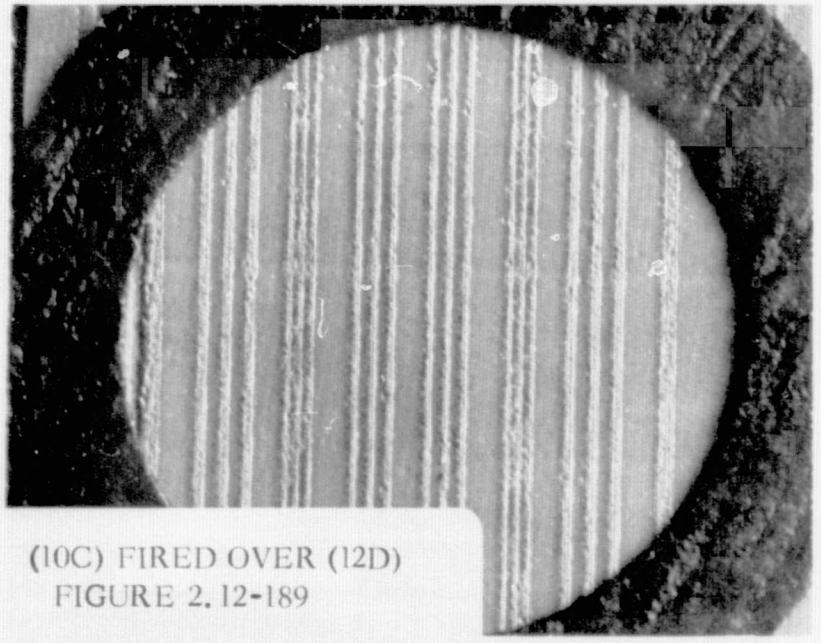
(10C) FIRED OVER (9D)
FIGURE 2.12-186



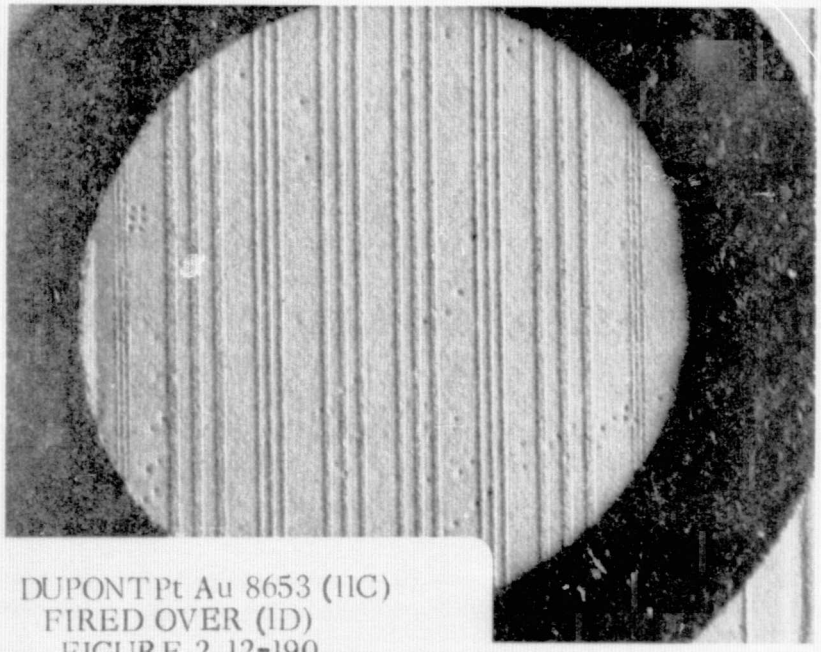
(10C) FIRED OVER (10D)
FIGURE 2.12-187



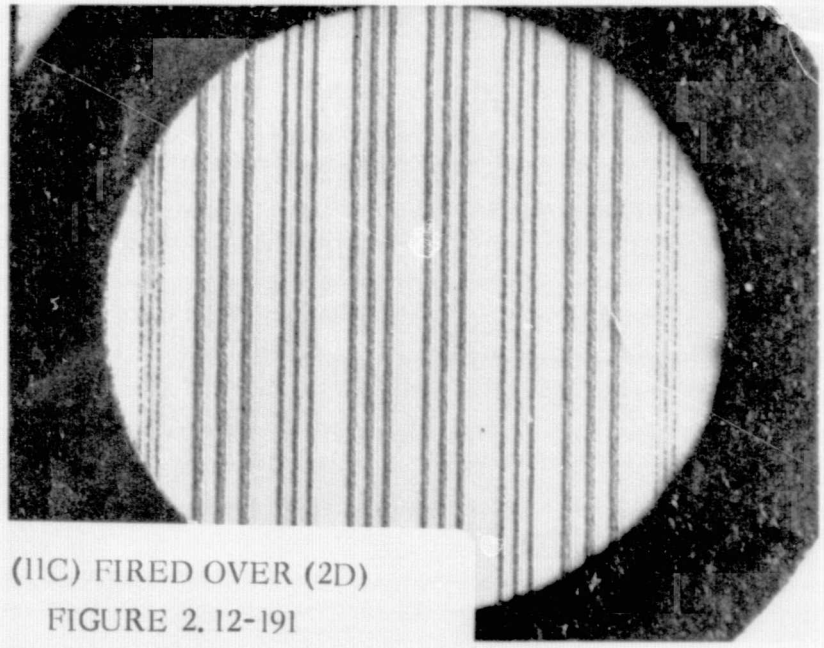
(10C) FIRED OVER (11D)
FIGURE 2.12-188



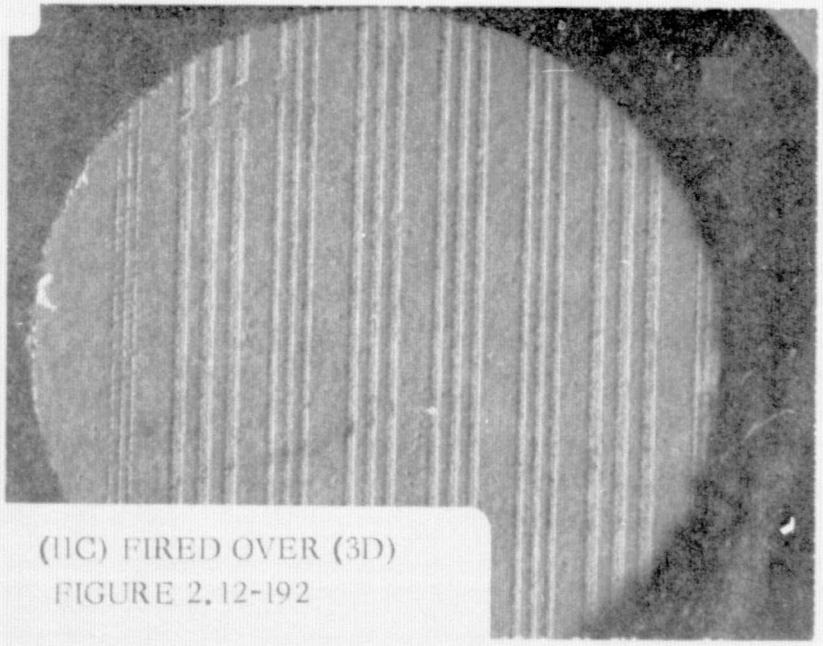
(10C) FIRED OVER (12D)
FIGURE 2.12-189



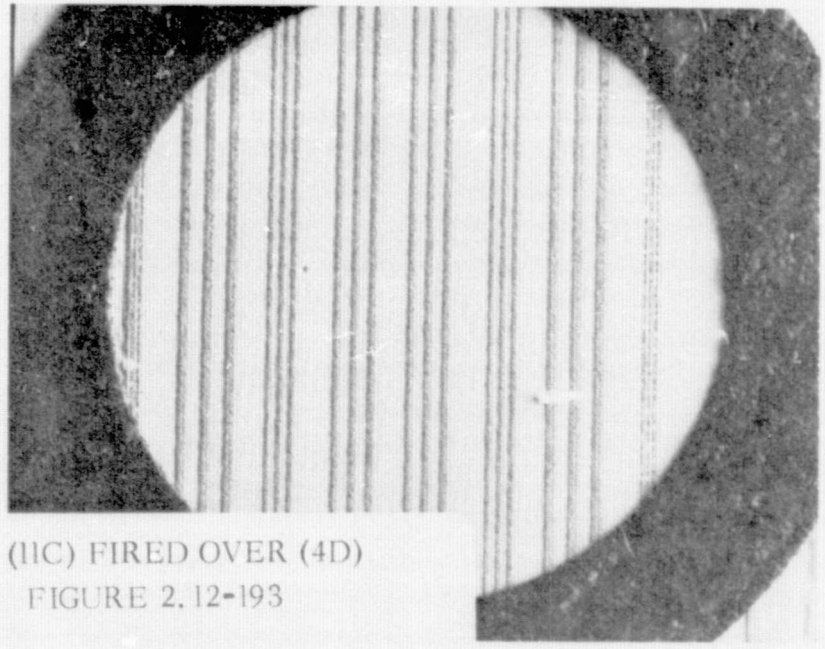
DUPONT Pt Au 8653 (11C)
FIRED OVER (1D)
FIGURE 2.12-190



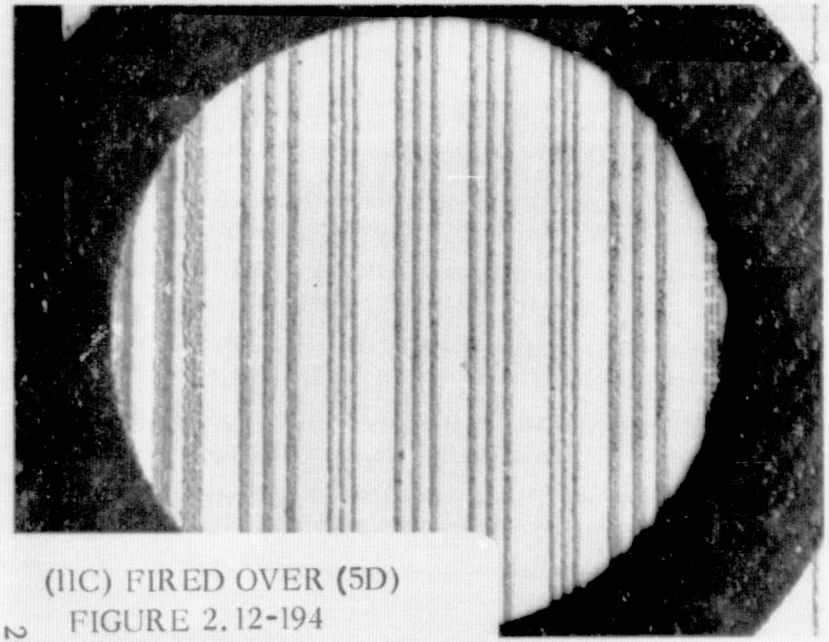
(11C) FIRED OVER (2D)
FIGURE 2.12-191



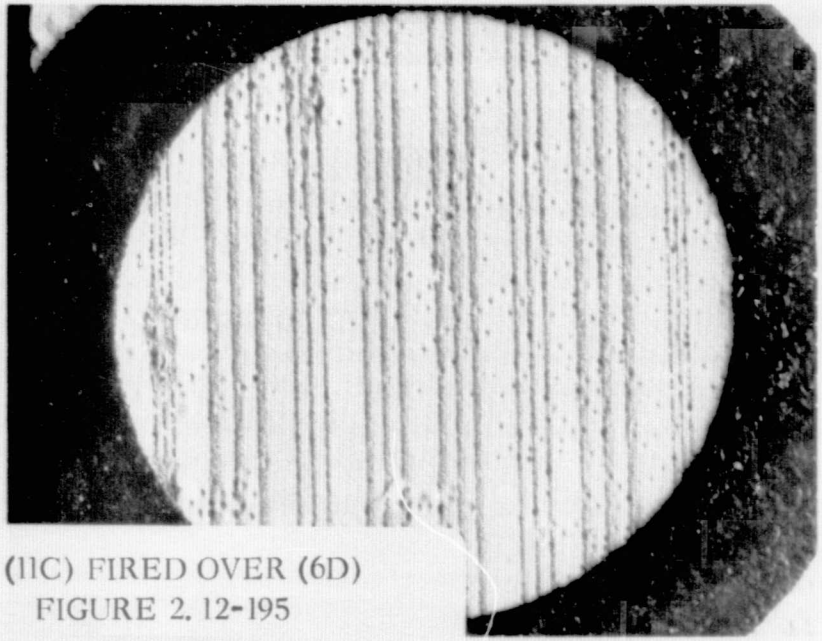
(11C) FIRED OVER (3D)
FIGURE 2.12-192



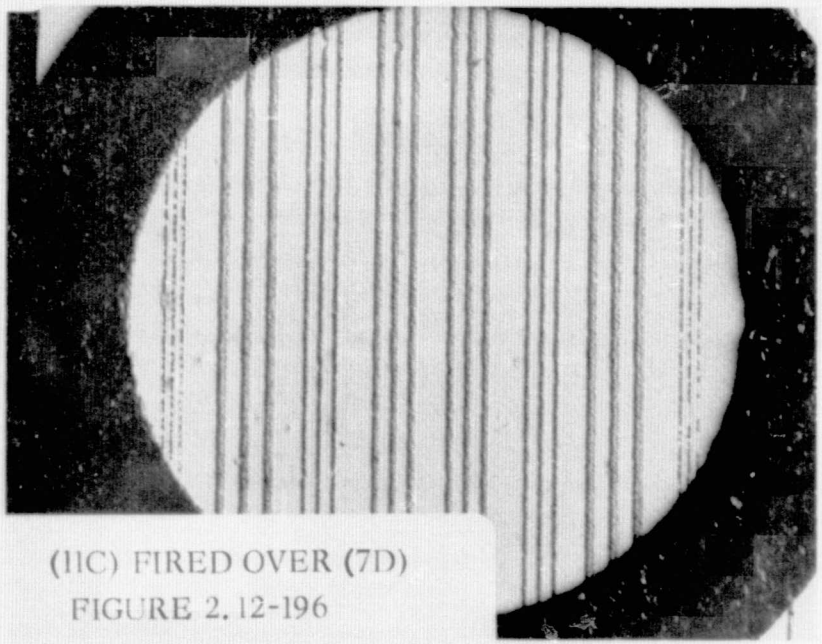
(11C) FIRED OVER (4D)
FIGURE 2.12-193



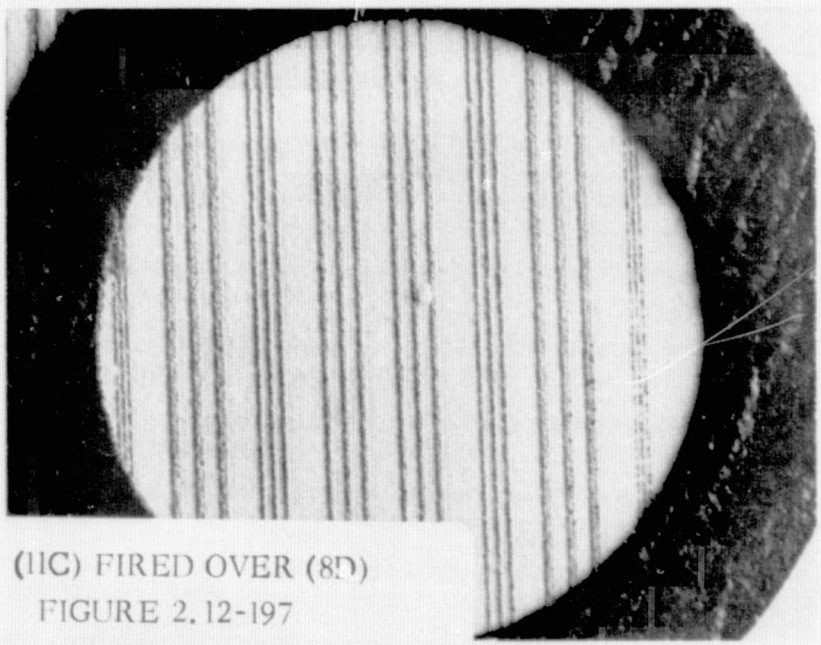
(11C) FIRED OVER (5D)
FIGURE 2.12-194



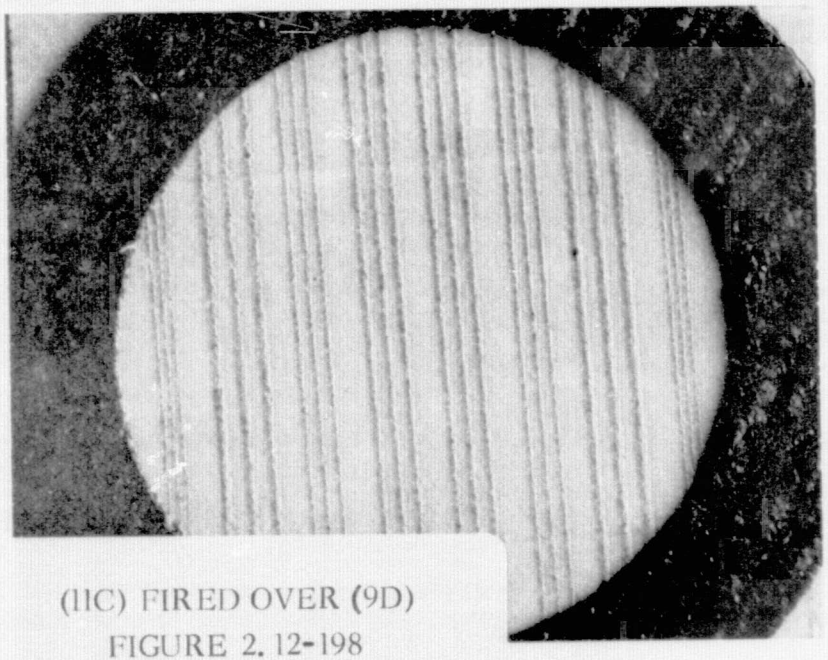
(11C) FIRED OVER (6D)
FIGURE 2.12-195



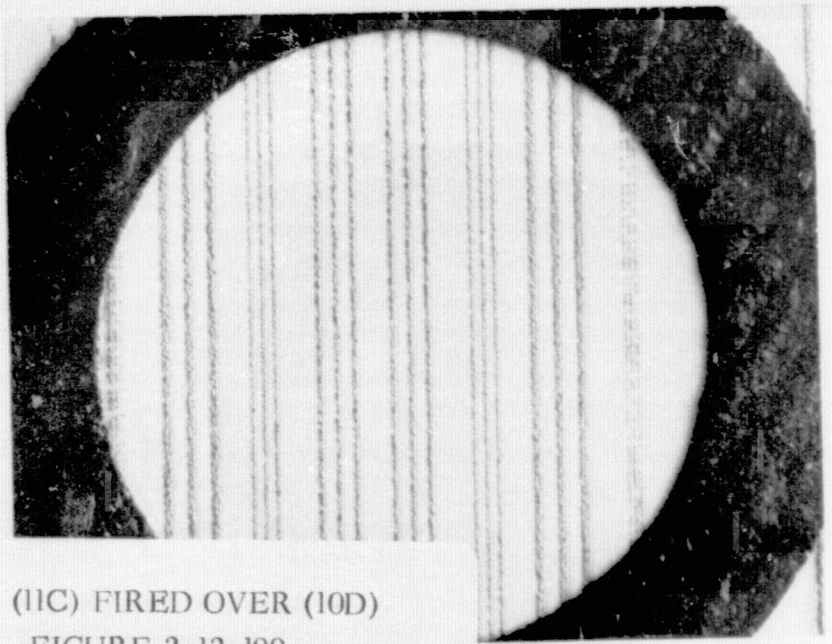
(11C) FIRED OVER (7D)
FIGURE 2.12-196



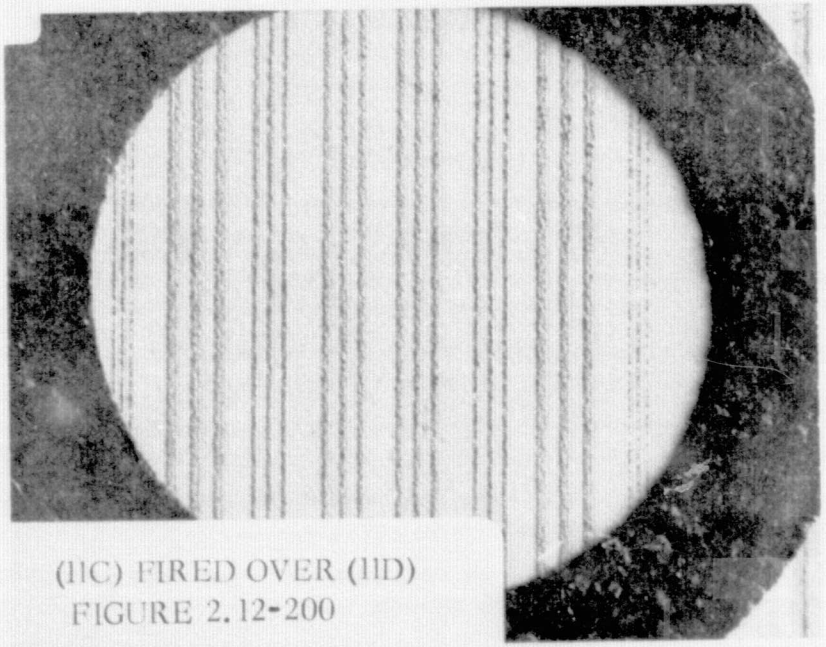
(11C) FIRED OVER (8D)
FIGURE 2.12-197



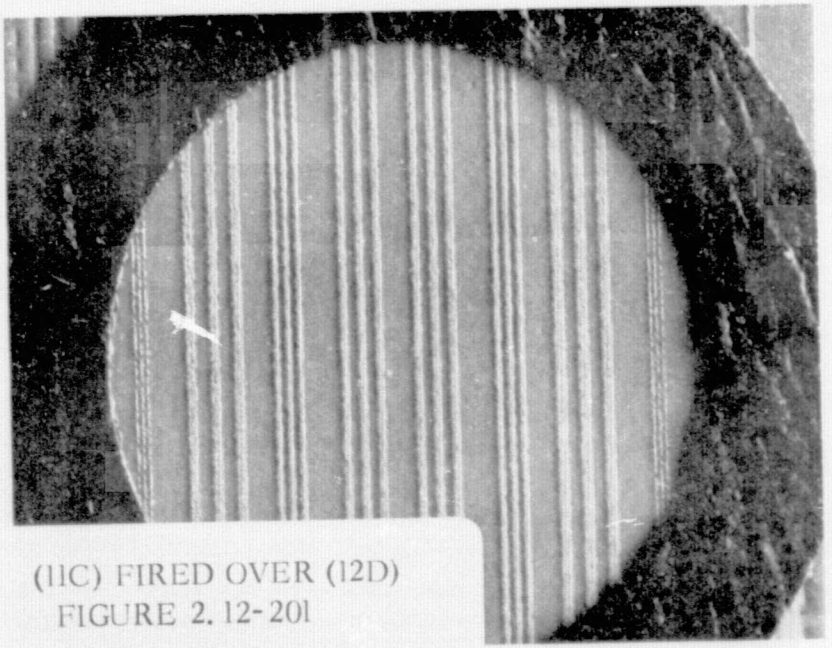
(11C) FIRED OVER (9D)
FIGURE 2.12-198



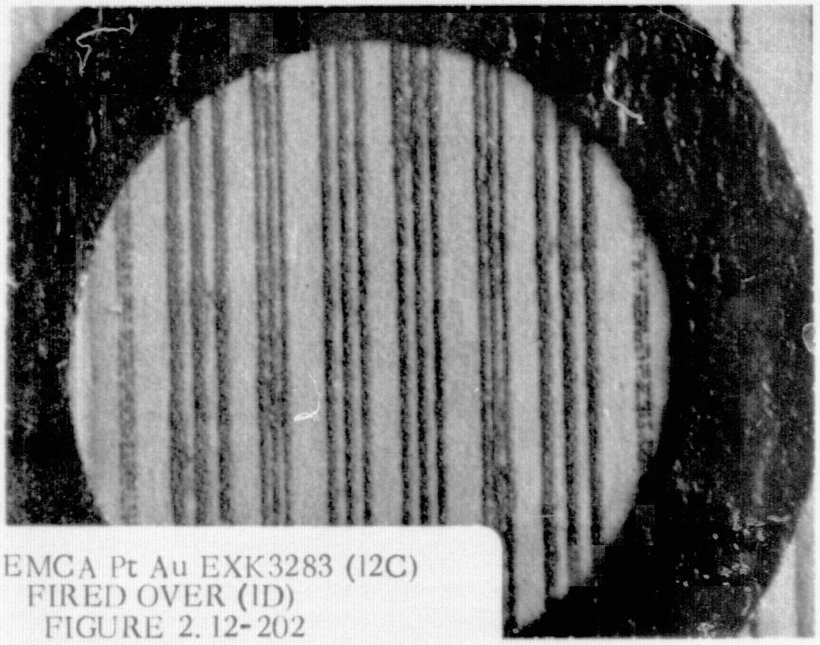
(11C) FIRED OVER (10D)
FIGURE 2.12-199



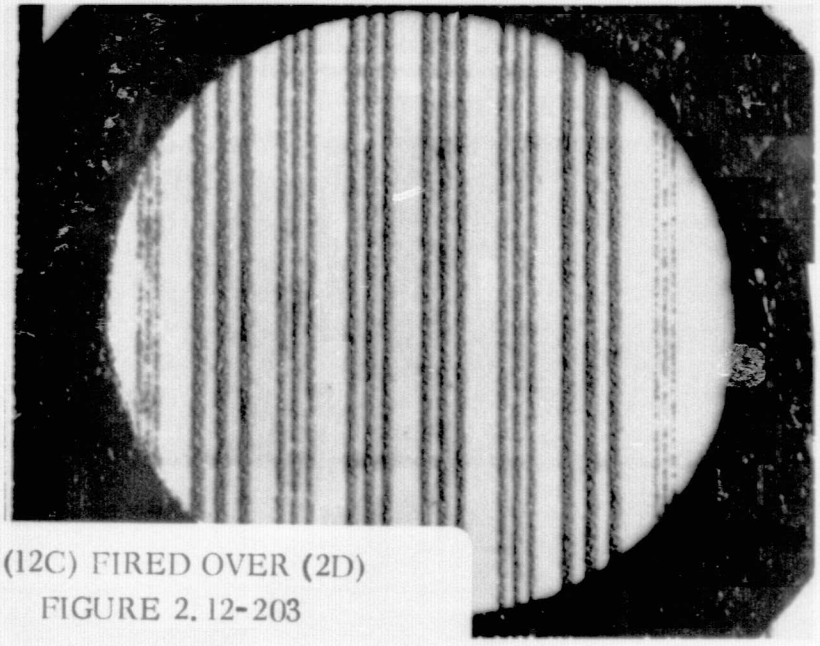
(11C) FIRED OVER (11D)
FIGURE 2.12-200



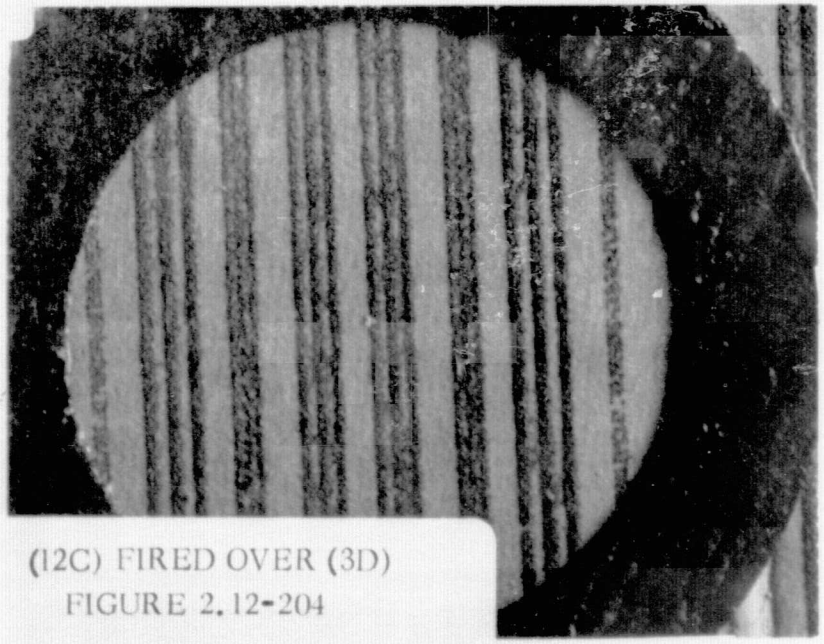
(11C) FIRED OVER (12D)
FIGURE 2.12-201



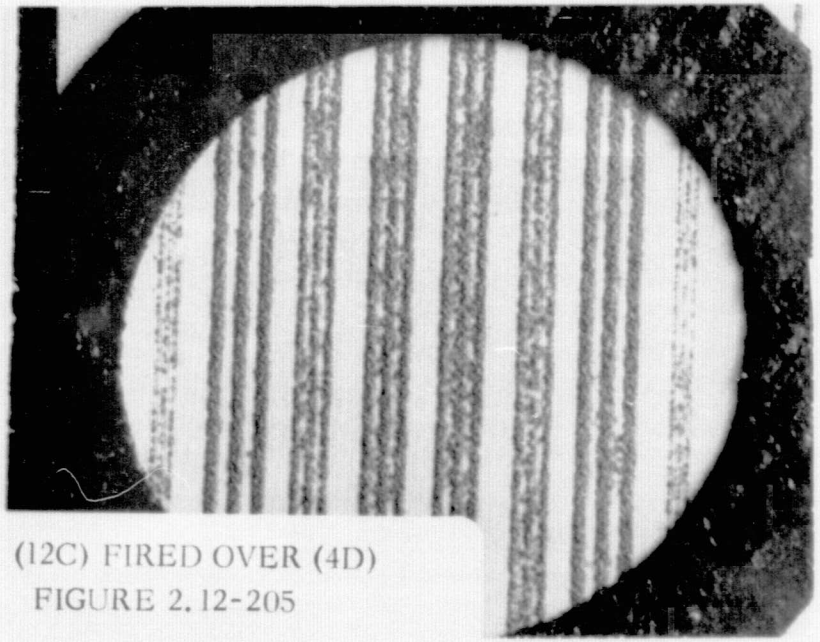
EMCA Pt Au EXK3283 (12C)
FIRED OVER (1D)
FIGURE 2.12-202



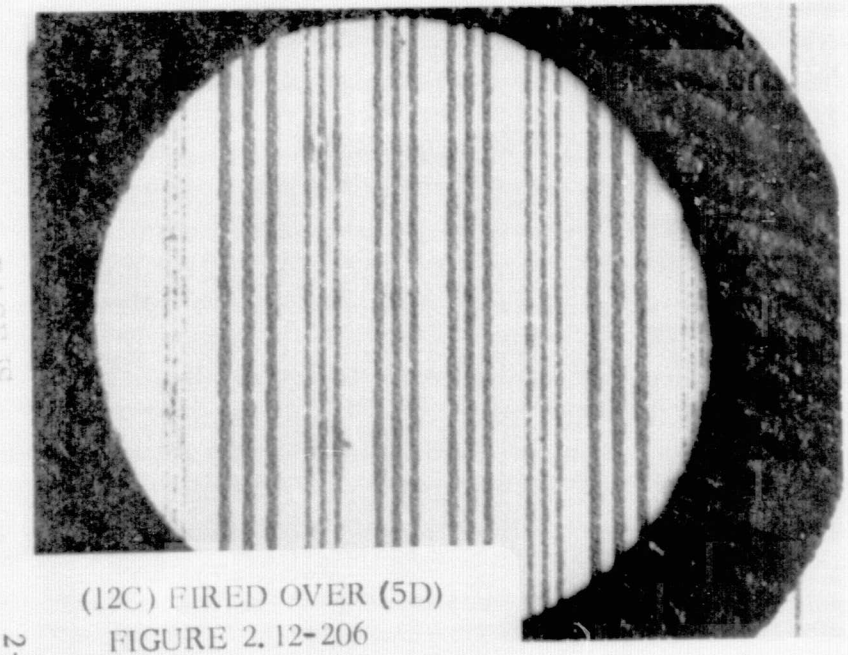
(12C) FIRED OVER (2D)
FIGURE 2.12-203



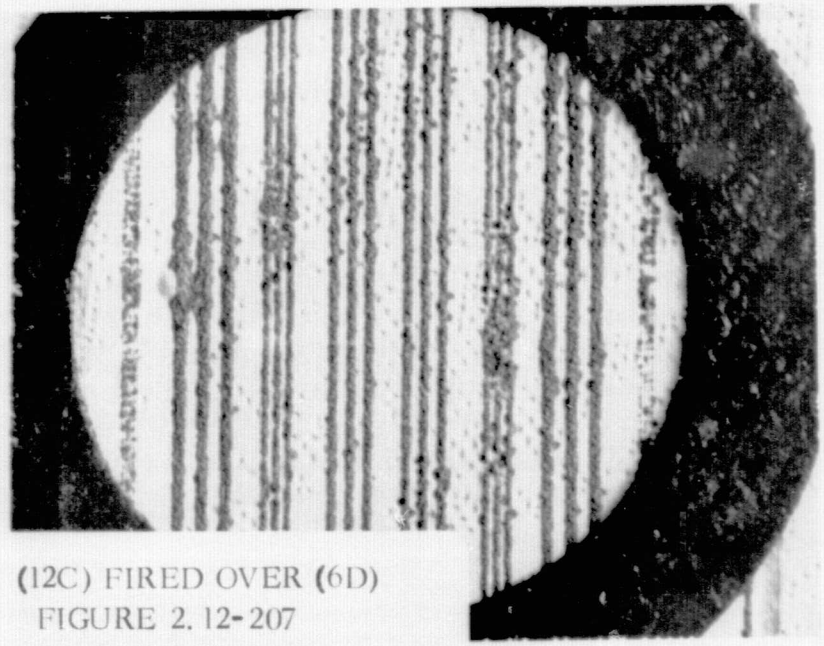
(12C) FIRED OVER (3D)
FIGURE 2.12-204



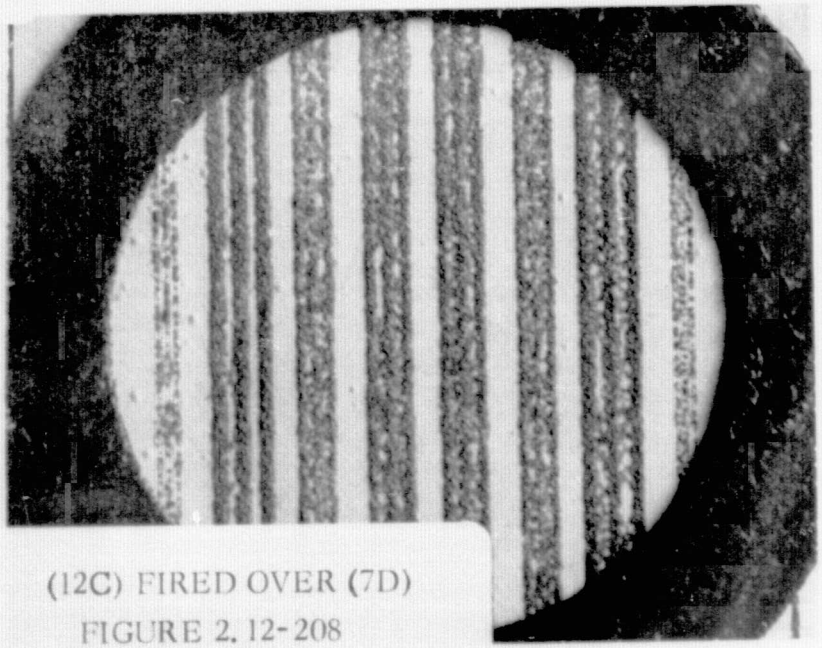
(12C) FIRED OVER (4D)
FIGURE 2.12-205



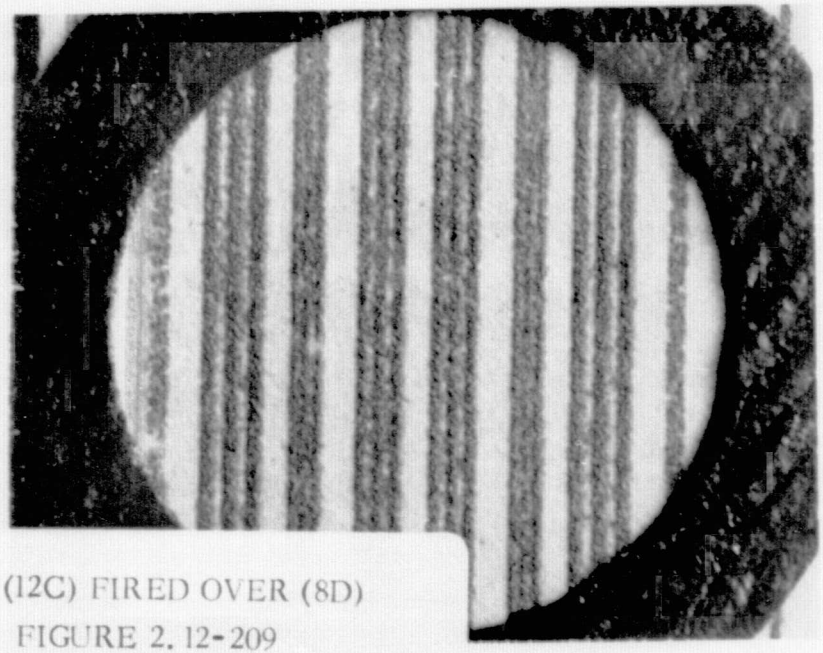
(12C) FIRED OVER (5D)
FIGURE 2. 12-206



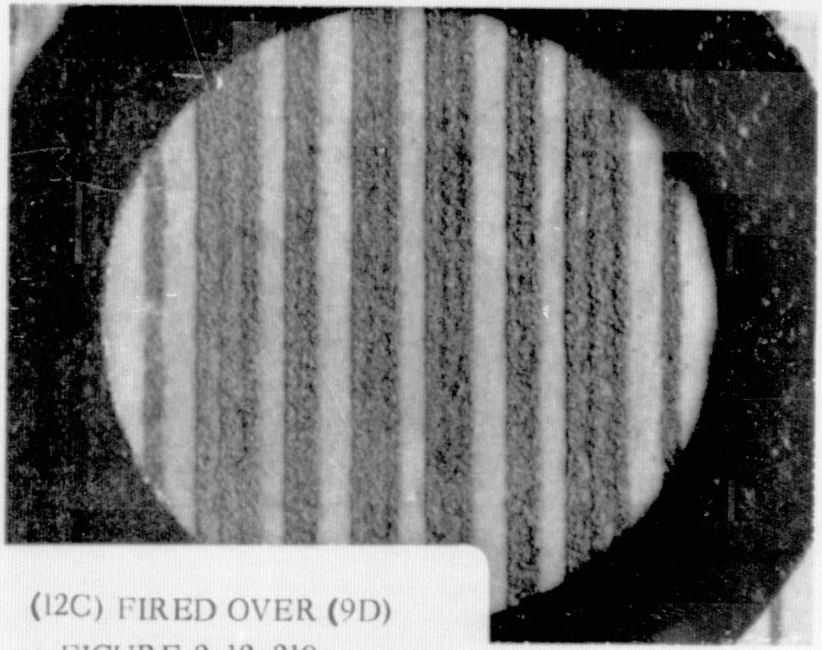
(12C) FIRED OVER (6D)
FIGURE 2. 12-207



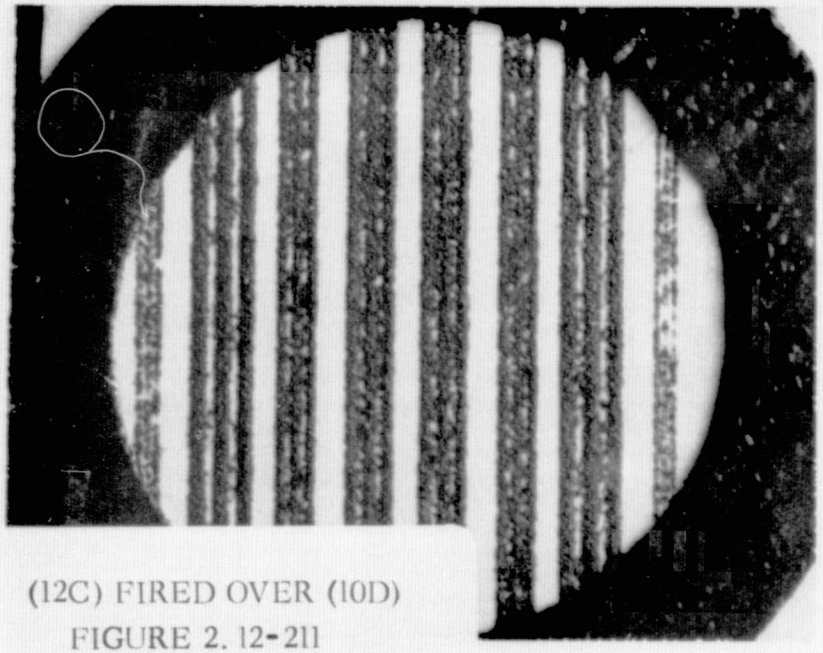
(12C) FIRED OVER (7D)
FIGURE 2. 12-208



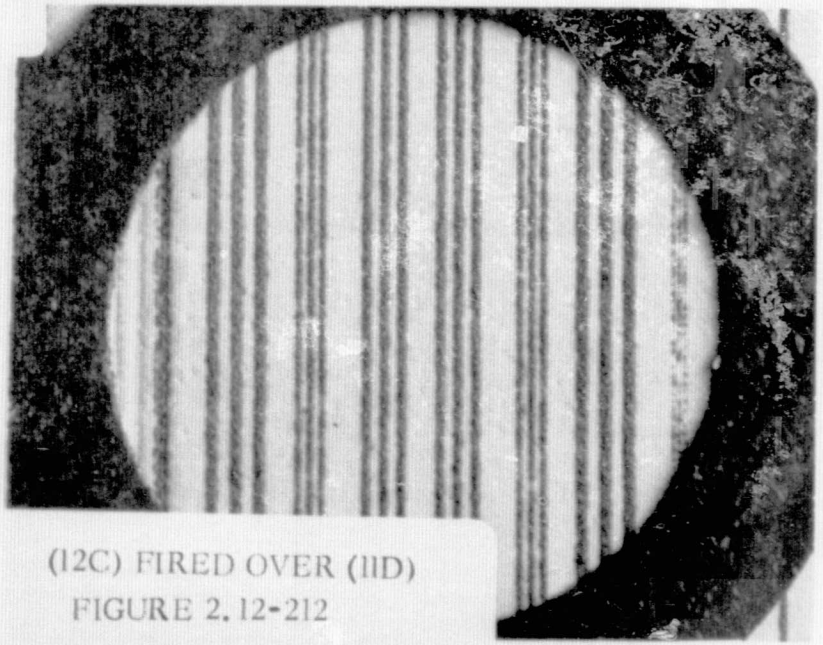
(12C) FIRED OVER (8D)
FIGURE 2. 12-209



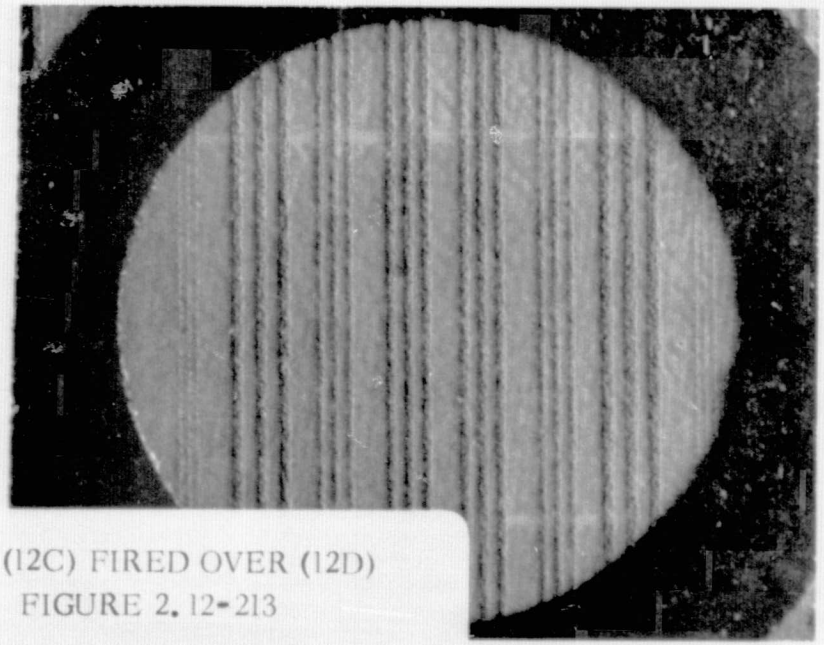
(12C) FIRED OVER (9D)
FIGURE 2.12-210



(12C) FIRED OVER (10D)
FIGURE 2.12-211

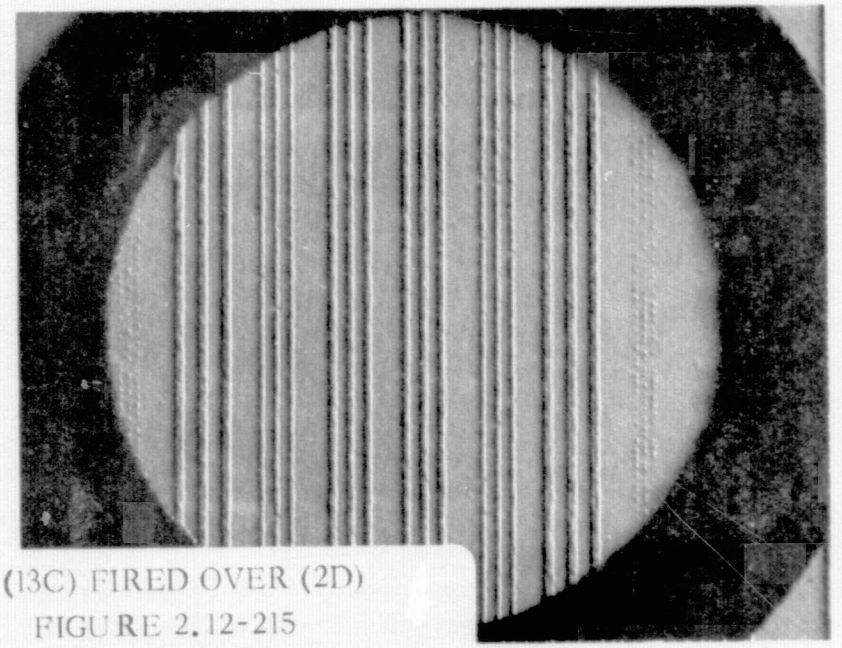


(12C) FIRED OVER (11D)
FIGURE 2.12-212

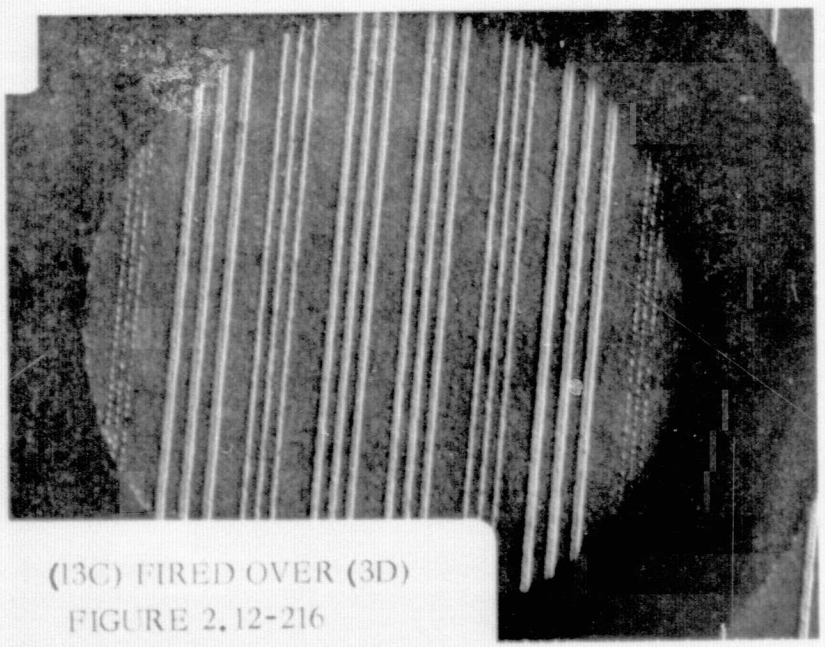


(12C) FIRED OVER (12D)
FIGURE 2.12-213

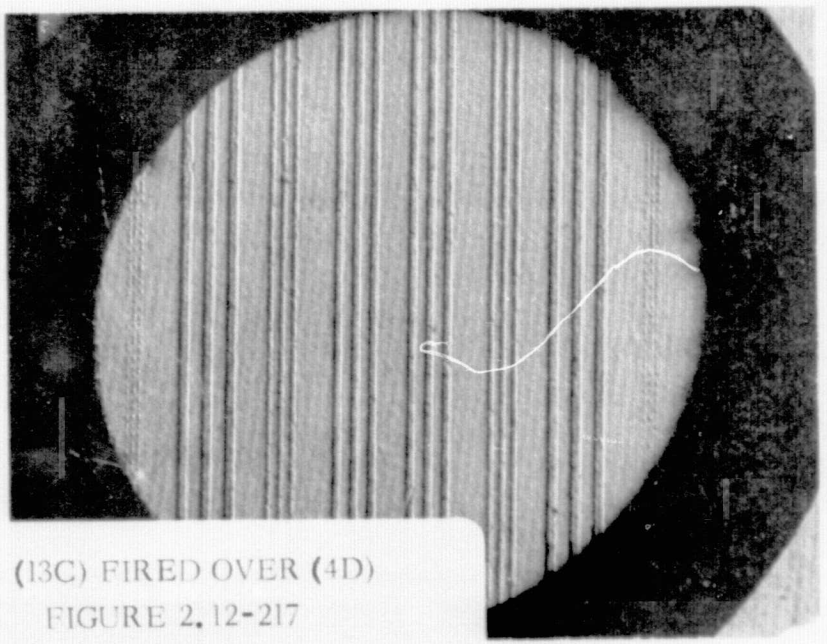
SEL-REX CO. GOLD DX-799
(13C) FIRED OVER (1D)
FIGURE 2.12-214



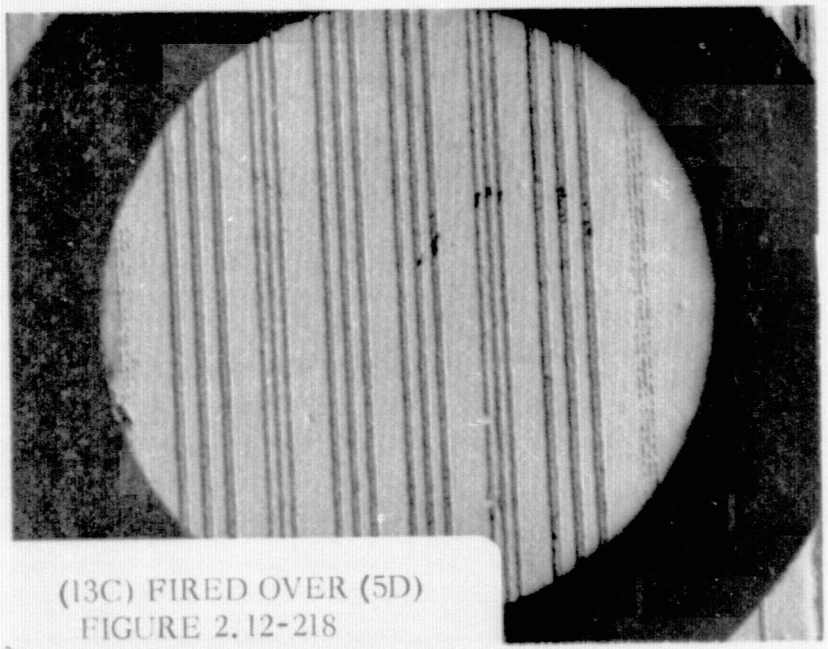
(13C) FIRED OVER (2D)
FIGURE 2.12-215



(13C) FIRED OVER (3D)
FIGURE 2.12-216

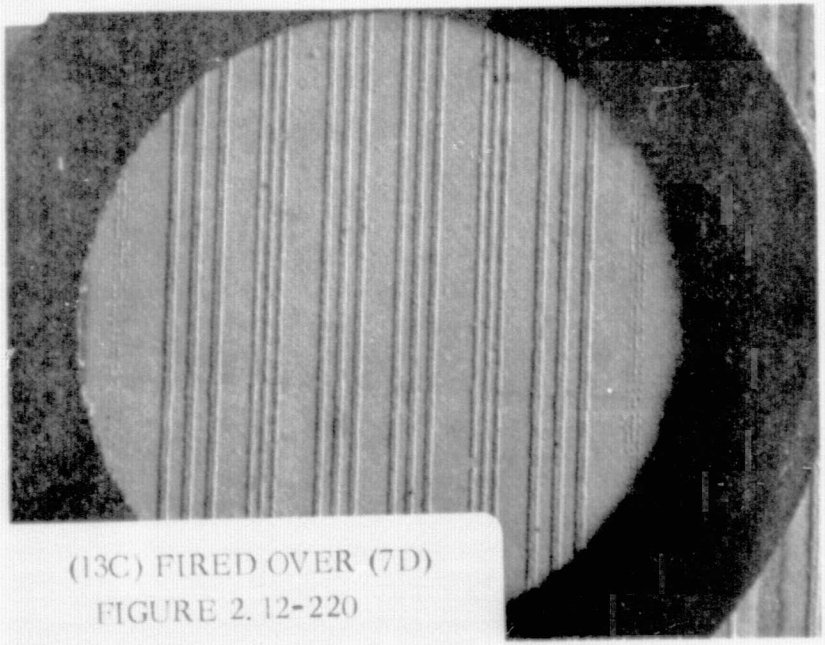


(13C) FIRED OVER (4D)
FIGURE 2.12-217



(13C) FIRED OVER (5D)
FIGURE 2.12-218

(13C) FIRED OVER (6D)
FIGURE 2.12-219



(13C) FIRED OVER (7D)
FIGURE 2.12-220

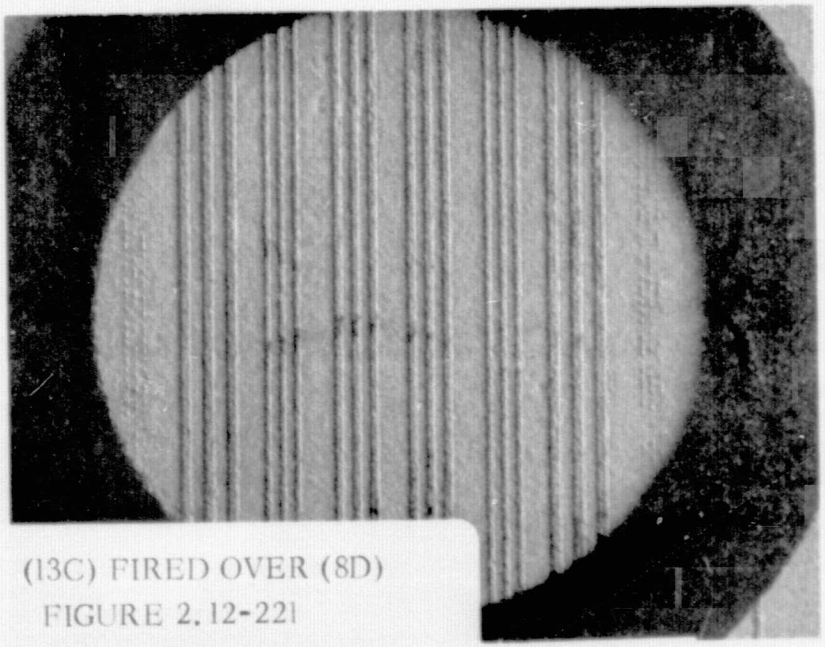


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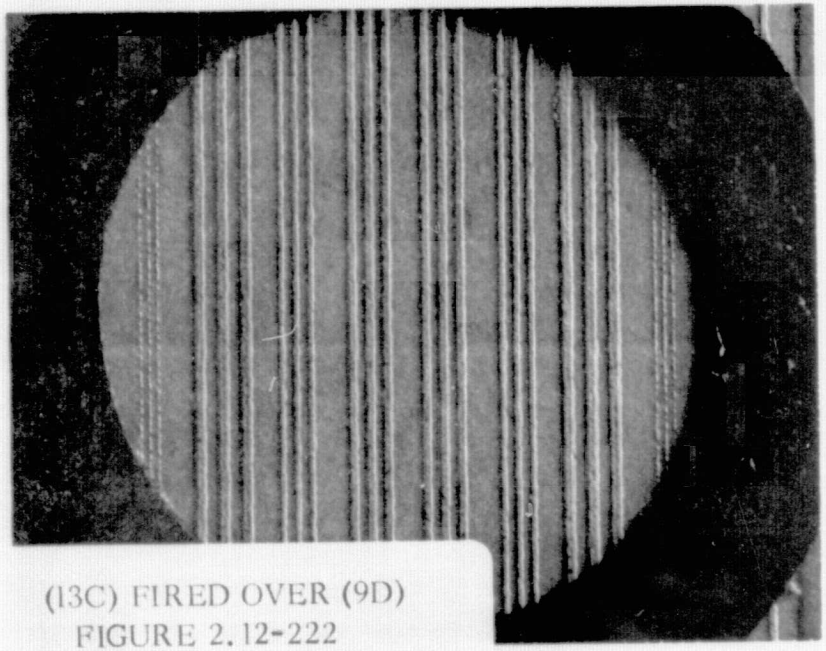
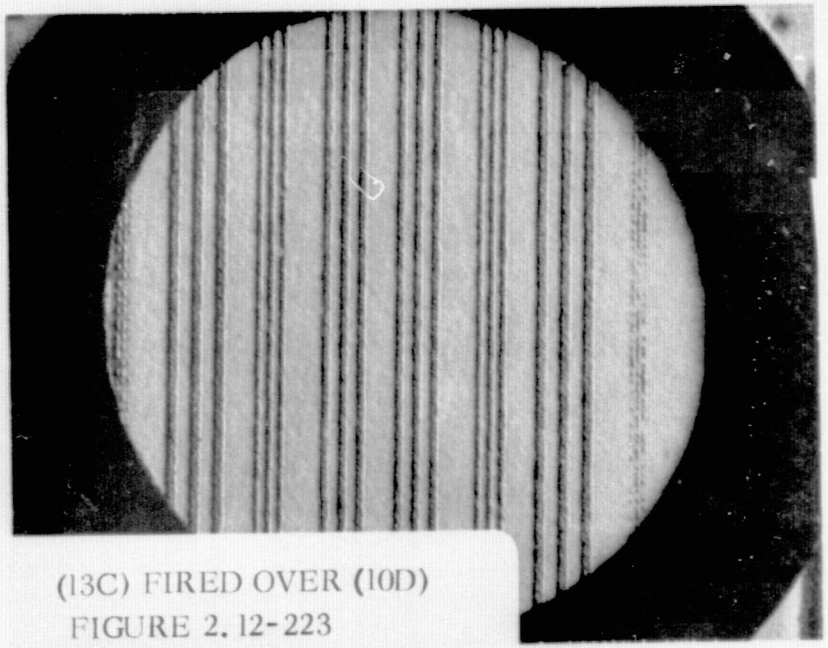
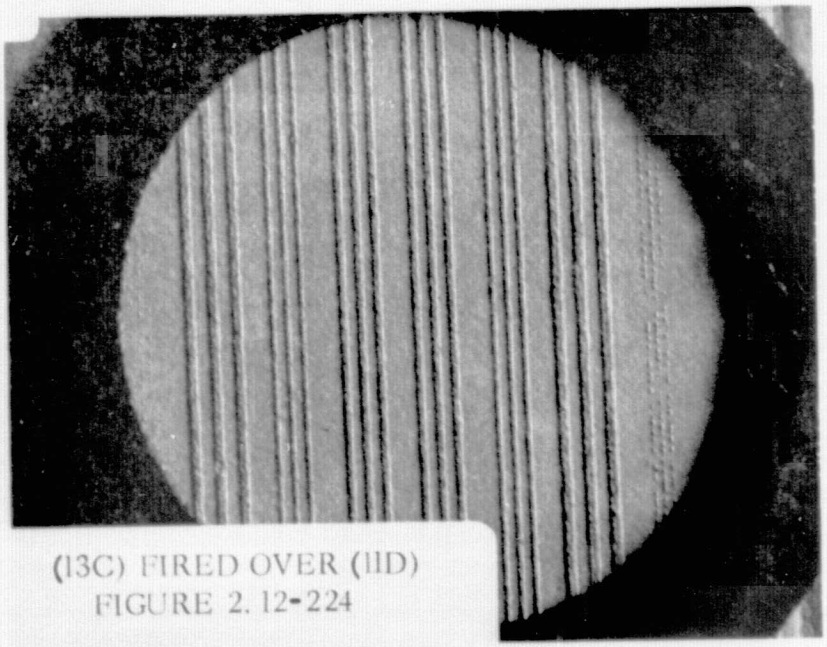
FIGURE 2.12-221



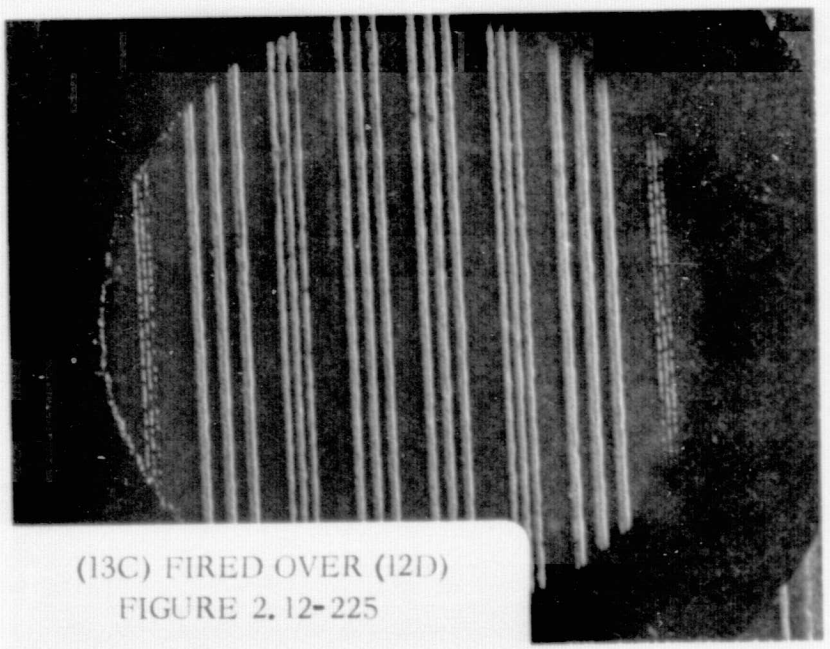
(13C) FIRED OVER (9D)
FIGURE 2.12-222



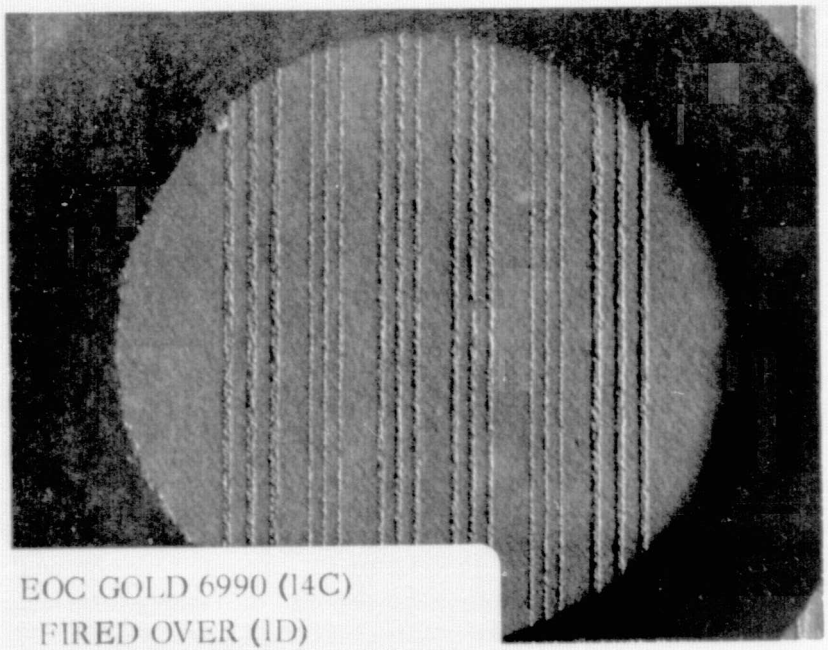
(13C) FIRED OVER (10D)
FIGURE 2.12-223



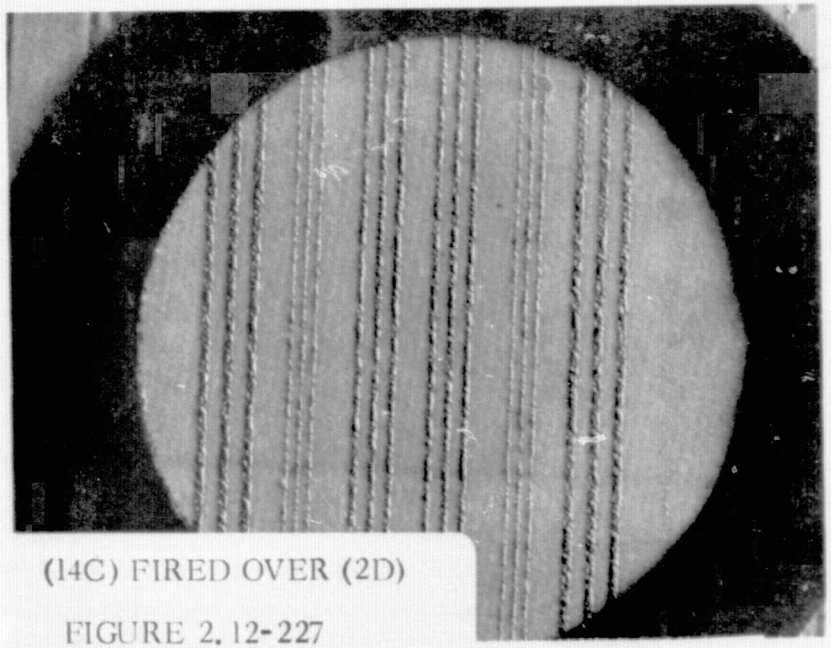
(13C) FIRED OVER (11D)
FIGURE 2.12-224



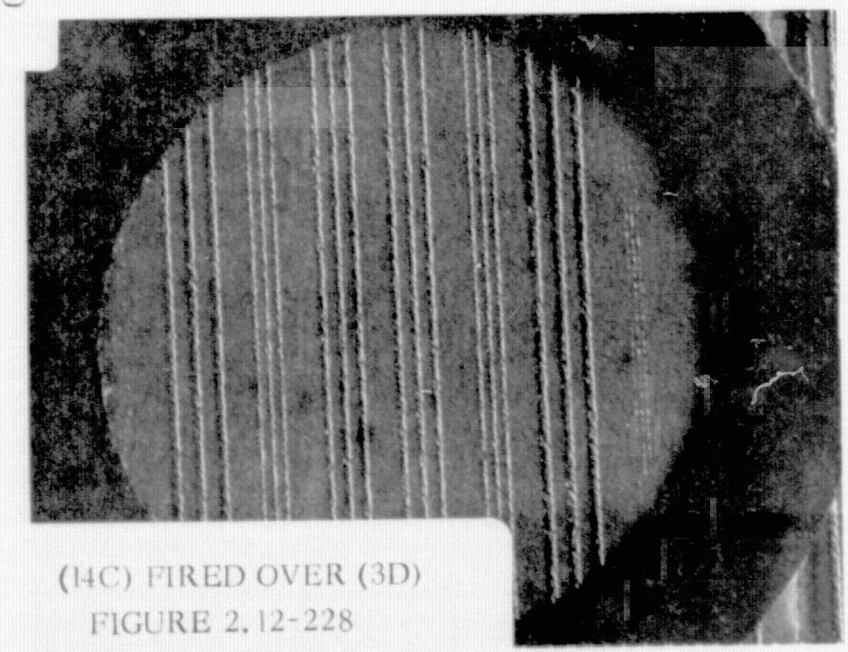
(13C) FIRED OVER (12D)
FIGURE 2.12-225



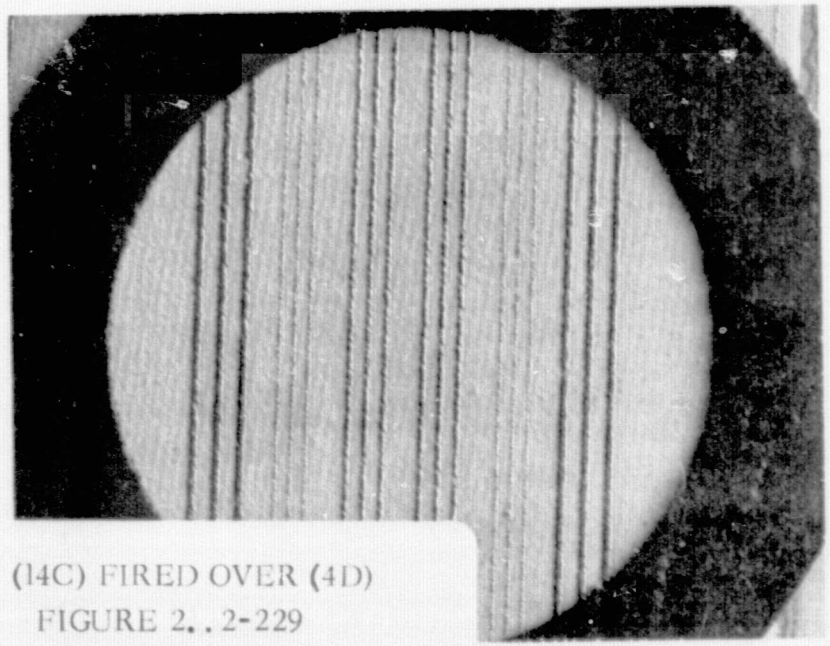
EOC GOLD 6990 (14C)
FIRED OVER (1D)
FIGURE 2.12-226



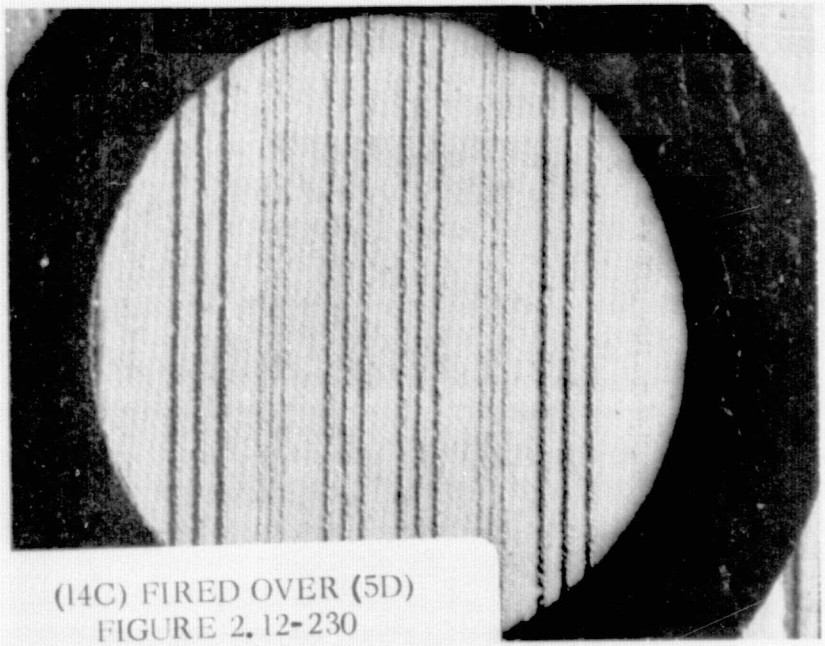
(14C) FIRED OVER (2D)
FIGURE 2.12-227



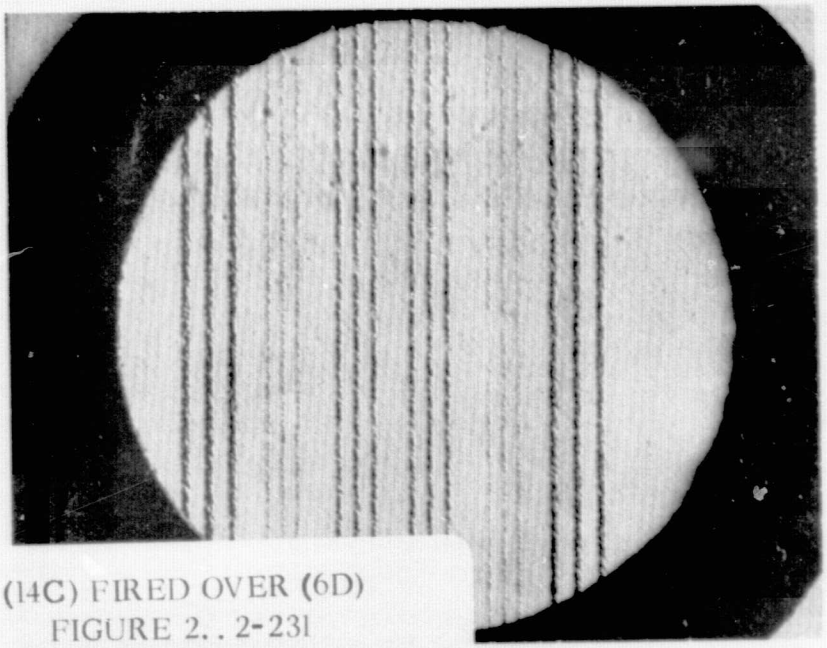
(14C) FIRED OVER (3D)
FIGURE 2.12-228



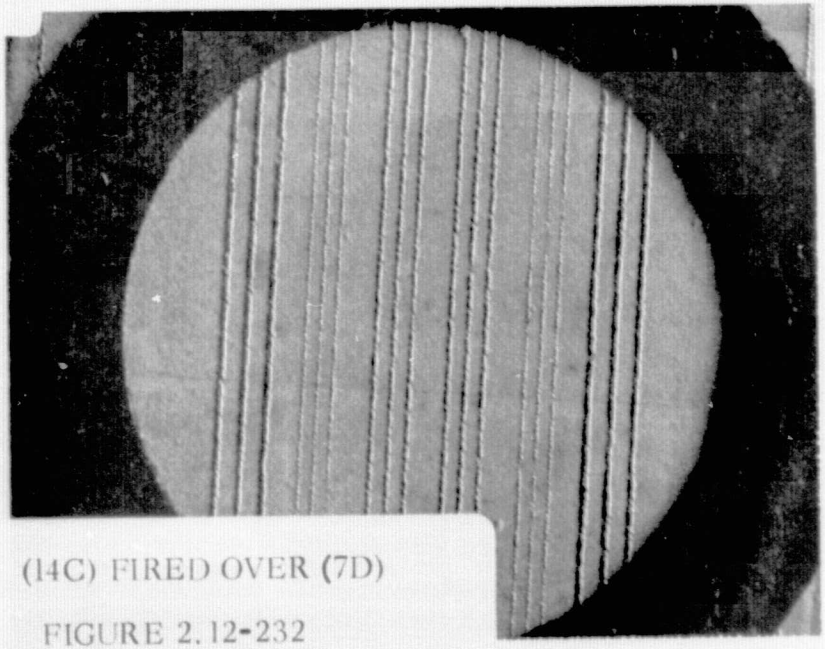
(14C) FIRED OVER (4D)
FIGURE 2.. 2-229



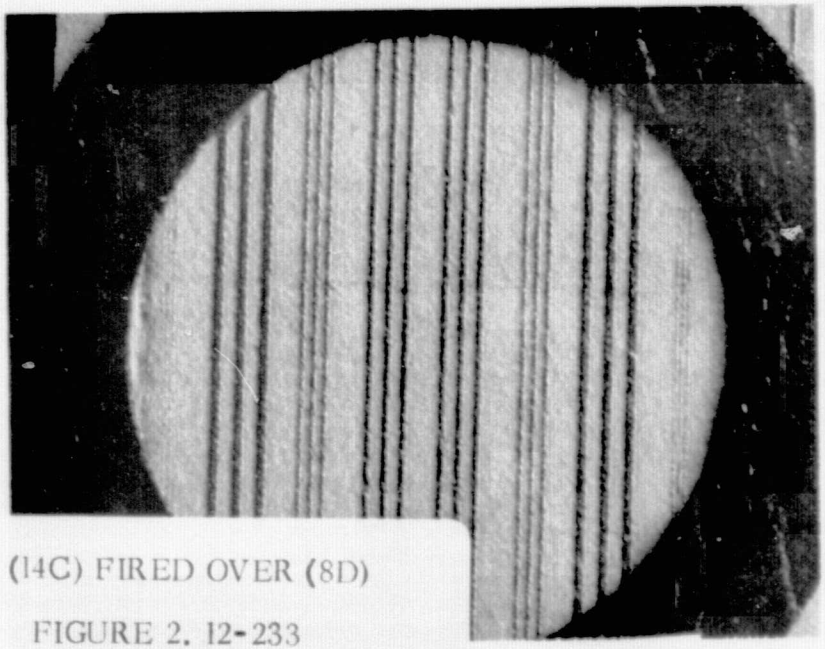
(14C) FIRED OVER (5D)
FIGURE 2.12-230



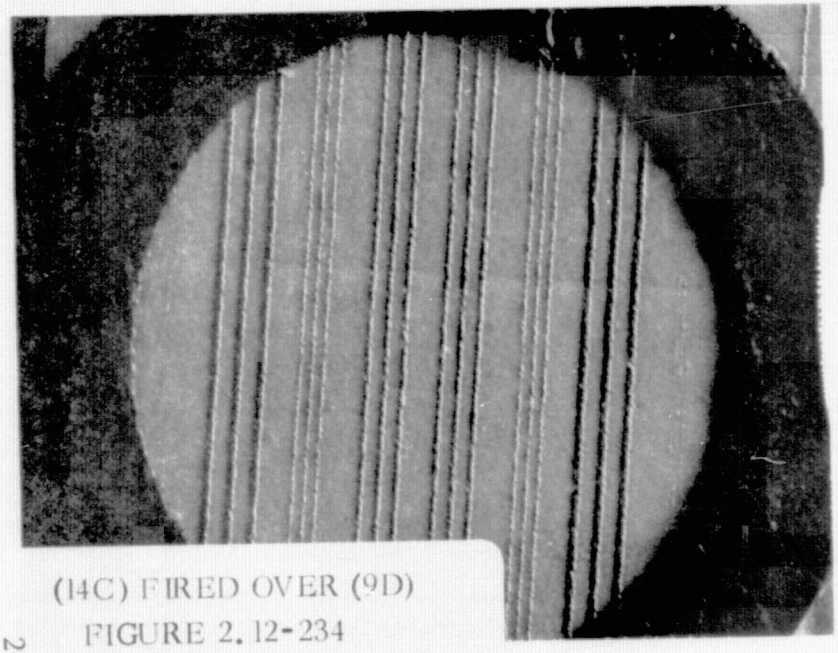
(14C) FIRED OVER (6D)
FIGURE 2..2-231



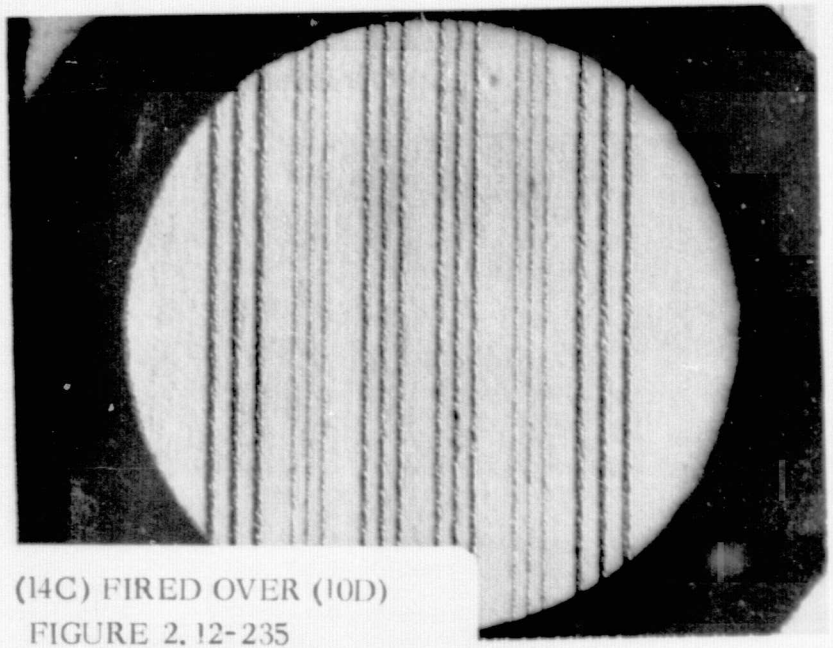
(14C) FIRED OVER (7D)
FIGURE 2.12-232



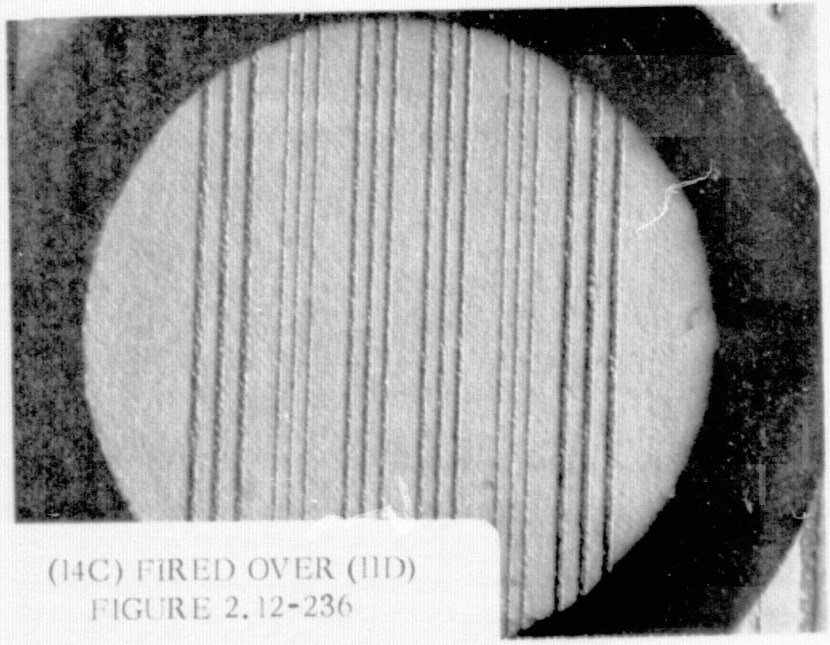
(14C) FIRED OVER (8D)
FIGURE 2. 12-233



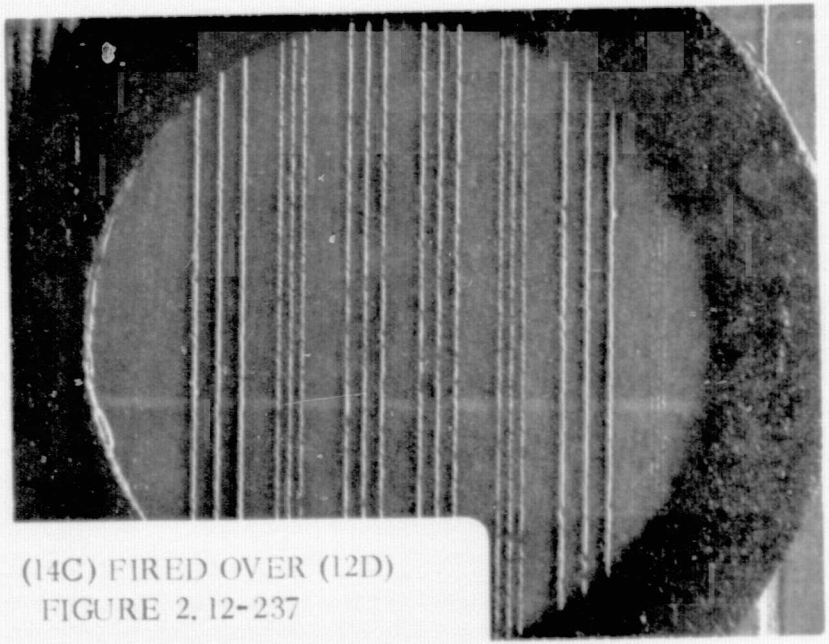
(14C) FIRED OVER (9D)
FIGURE 2.12-234



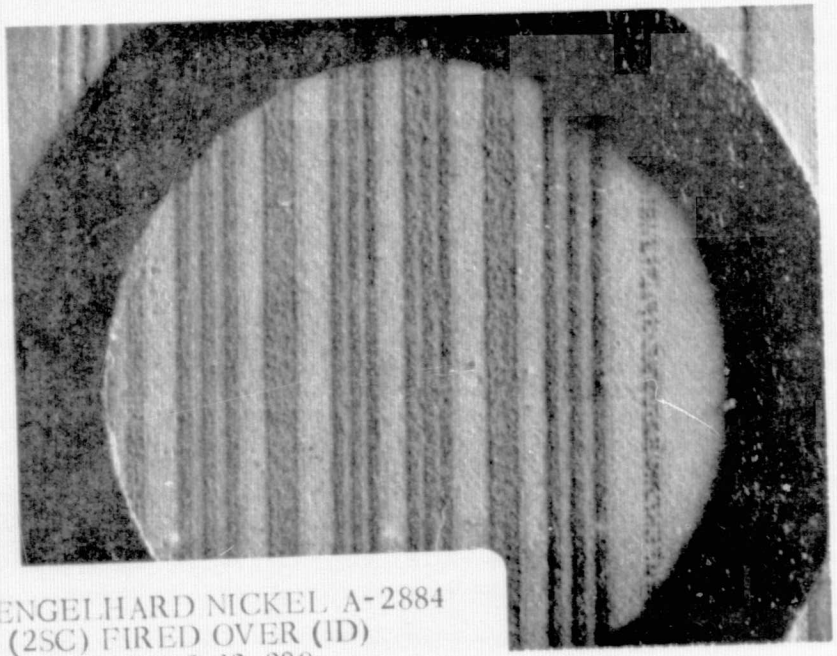
(14C) FIRED OVER (10D)
FIGURE 2.12-235



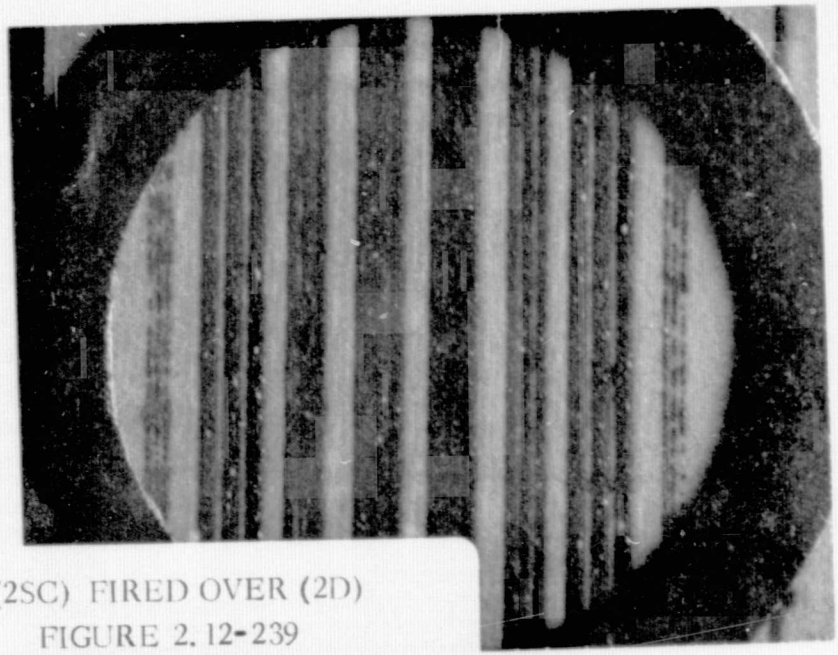
(14C) FIRED OVER (11D)
FIGURE 2.12-236



(14C) FIRED OVER (12D)
FIGURE 2.12-237

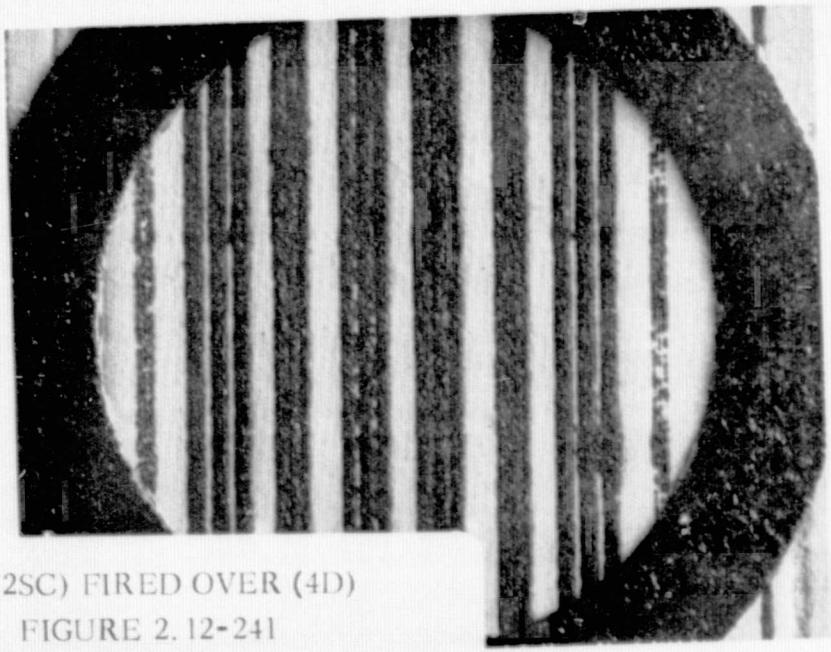


ENGELHARD NICKEL A-2884
(2SC) FIRED OVER (1D)
FIGURE 2.12-238

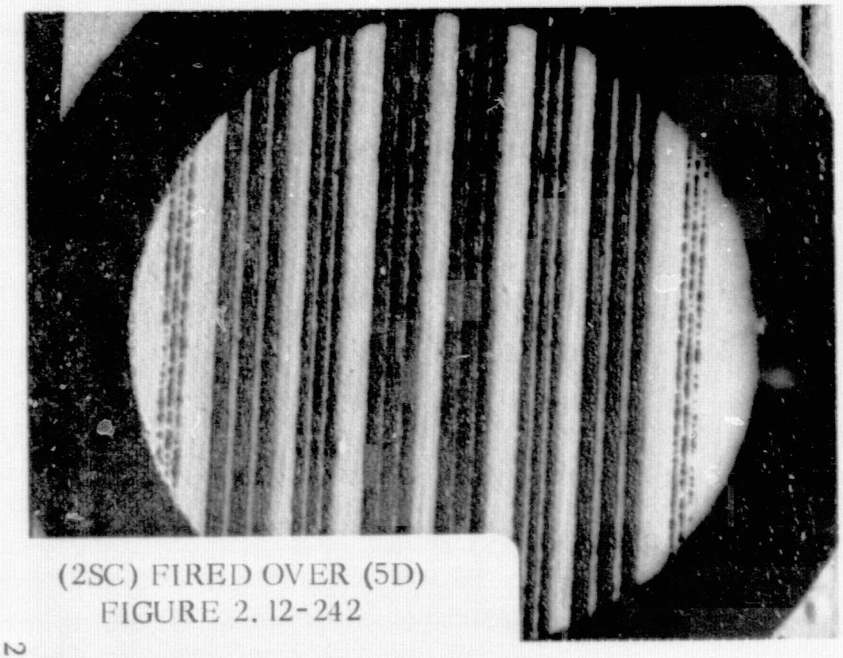


(2SC) FIRED OVER (2D)
FIGURE 2.12-239

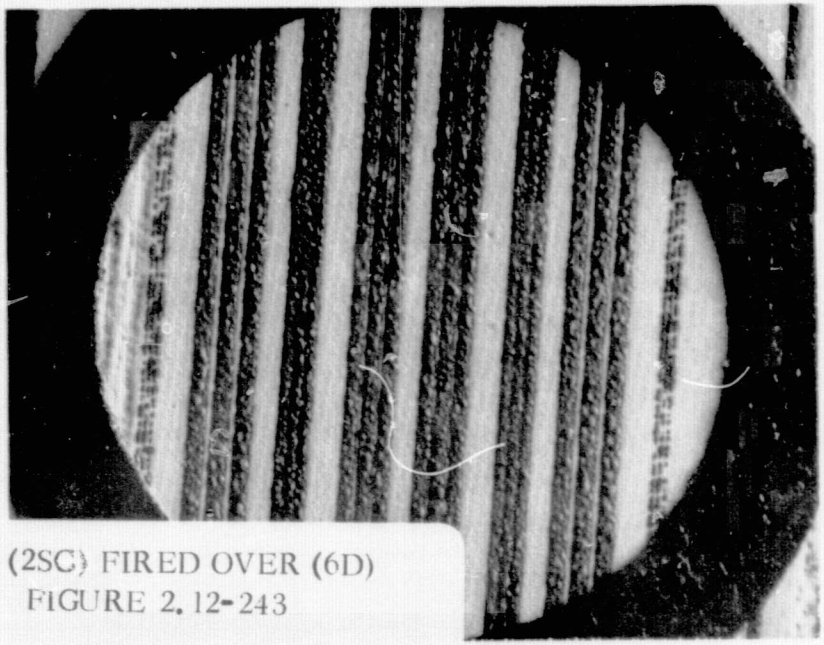
(2SC) FIRED OVER (3D)
FIGURE 2.12-240



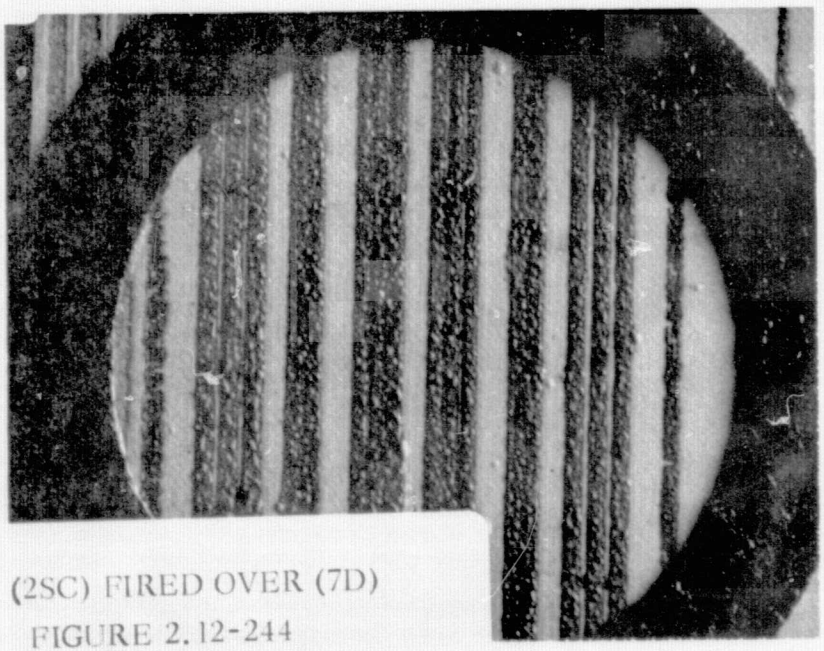
(2SC) FIRED OVER (4D)
FIGURE 2.12-241



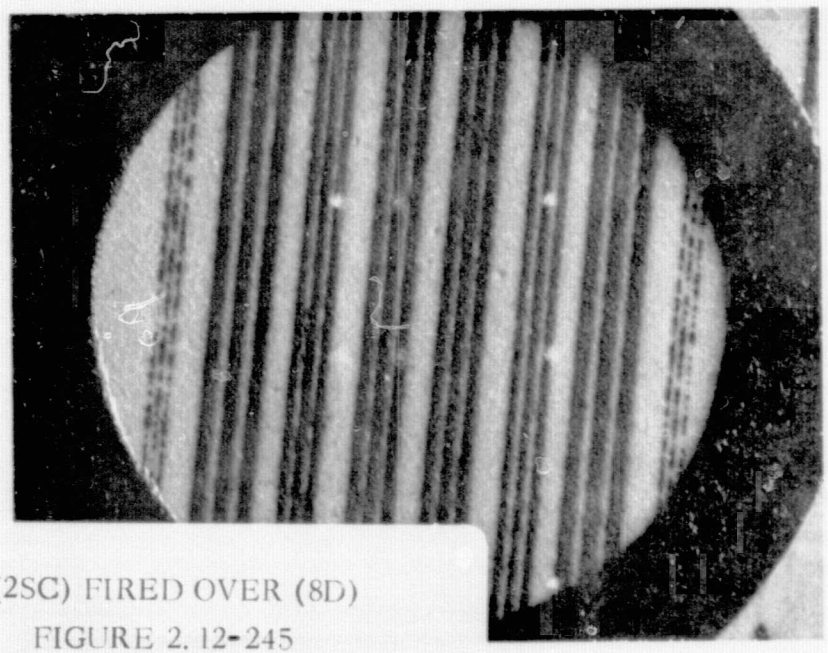
(2SC) FIRED OVER (5D)
FIGURE 2.12-242



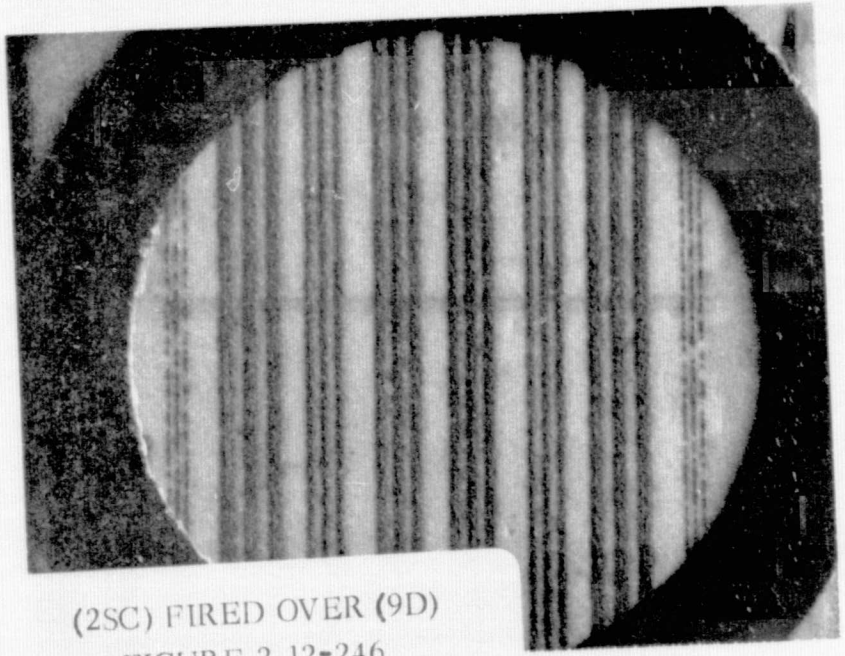
(2SC) FIRED OVER (6D)
FIGURE 2.12-243



(2SC) FIRED OVER (7D)
FIGURE 2.12-244

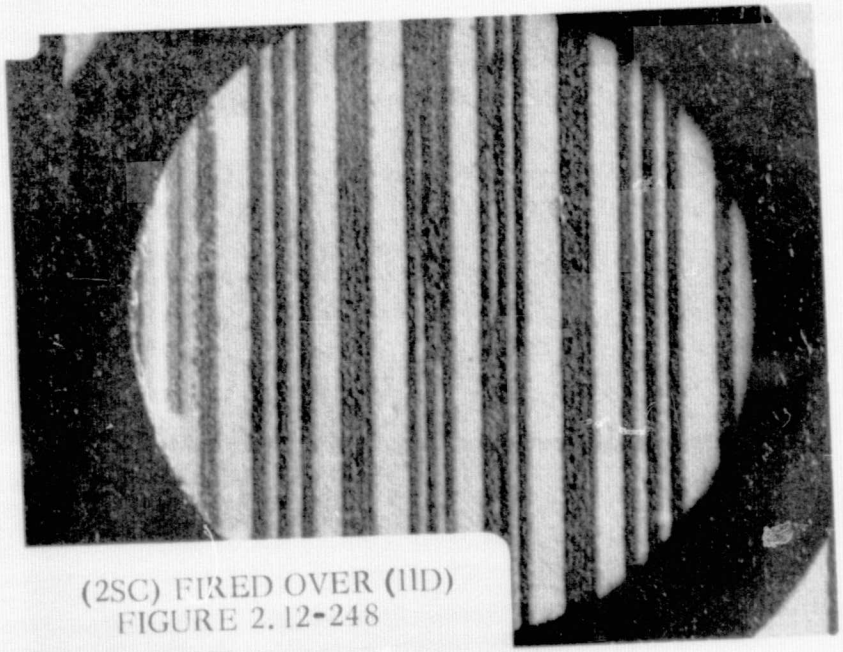


(2SC) FIRED OVER (8D)
FIGURE 2.12-245

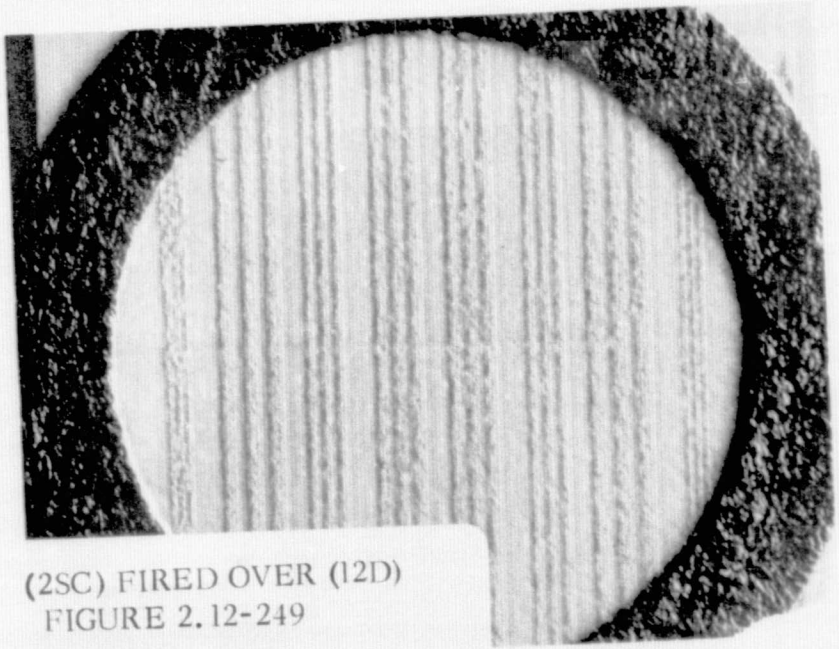


(2SC) FIRED OVER (9D)
FIGURE 2.12-246

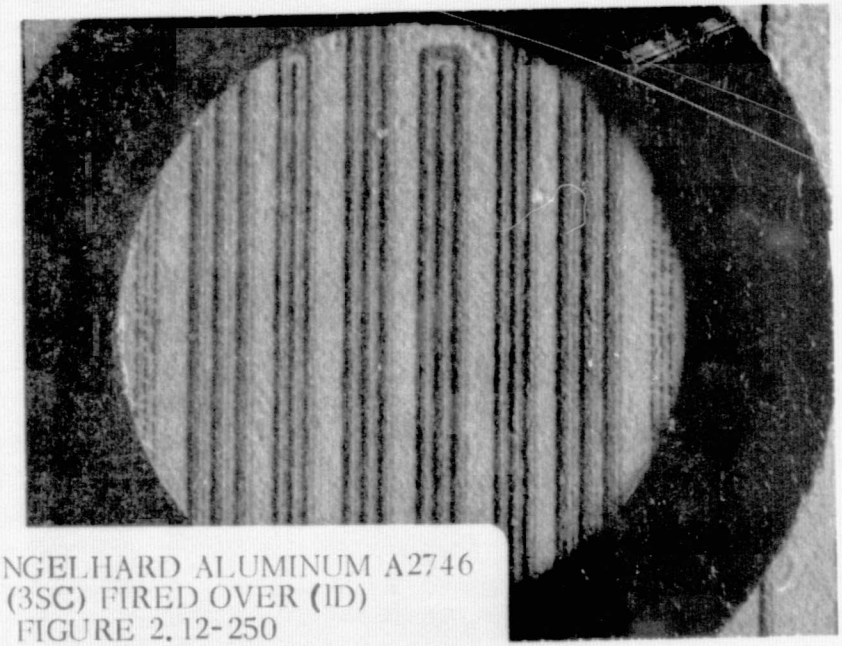
(2SC) FIRED OVER (10D)
FIGURE 2.12-247



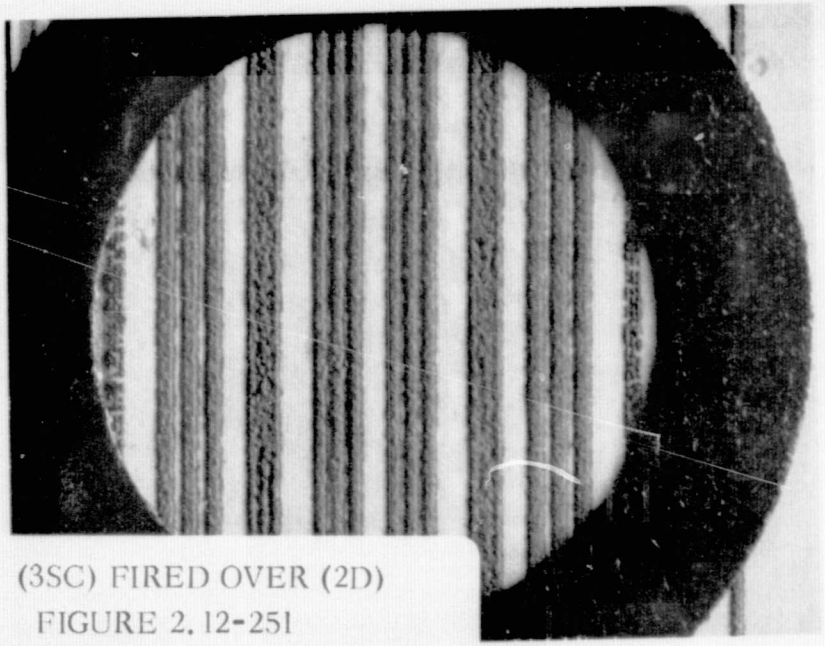
(2SC) FIRED OVER (11D)
FIGURE 2.12-248



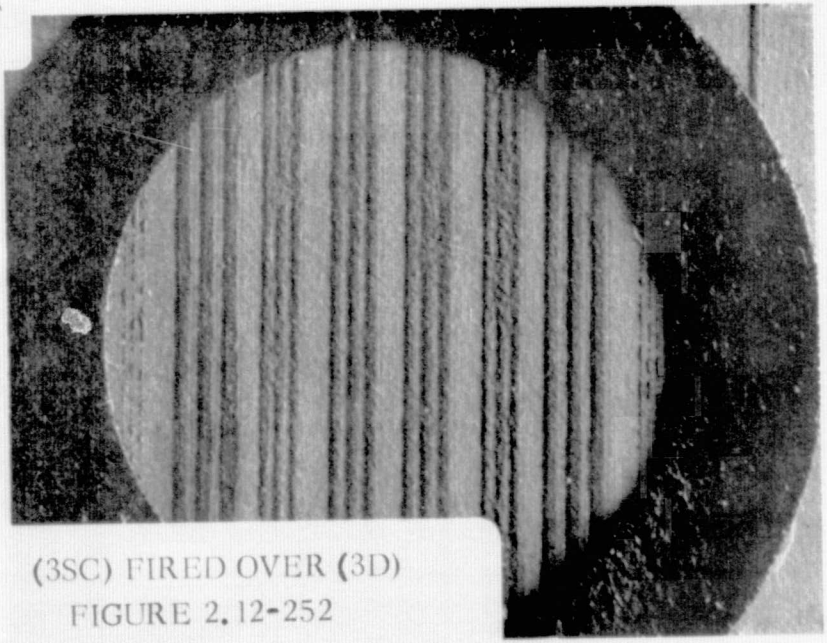
(2SC) FIRED OVER (12D)
FIGURE 2.12-249



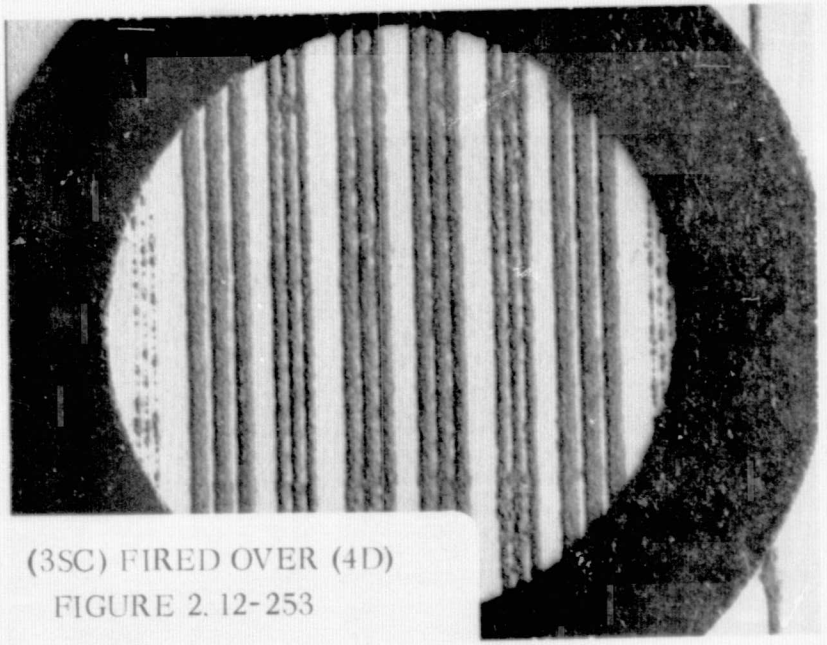
ENGELHARD ALUMINUM A2746
(3SC) FIRED OVER (1D)
FIGURE 2.12-250



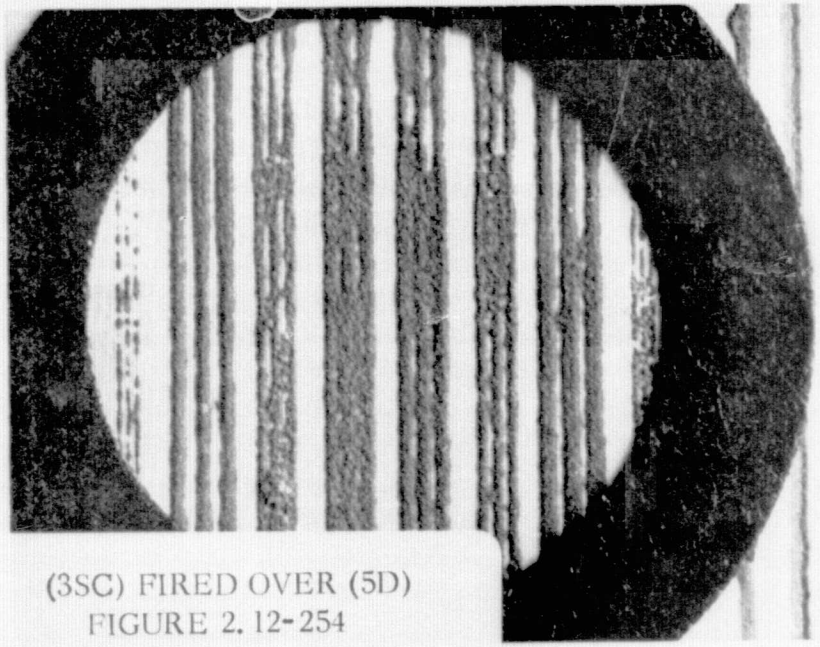
(3SC) FIRED OVER (2D)
FIGURE 2.12-251



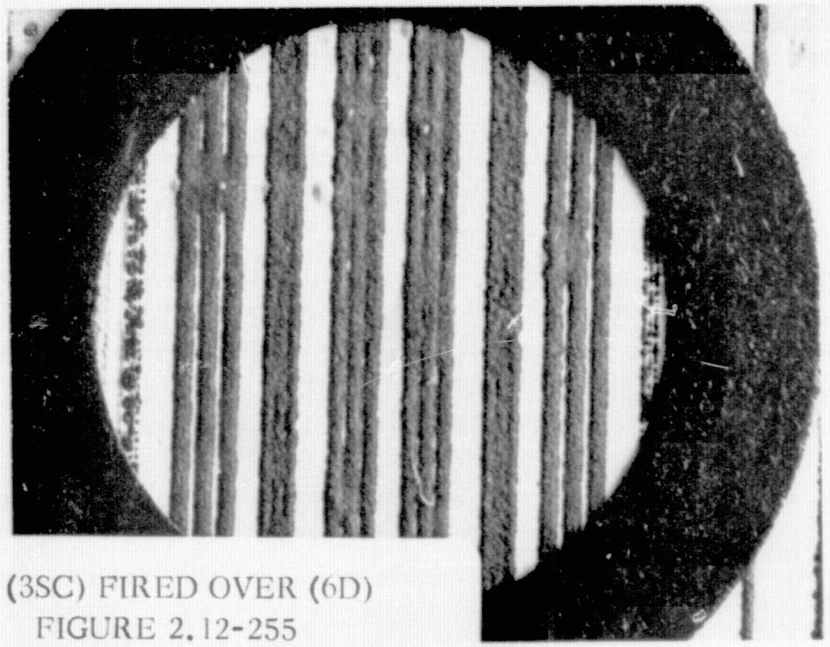
(3SC) FIRED OVER (3D)
FIGURE 2.12-252



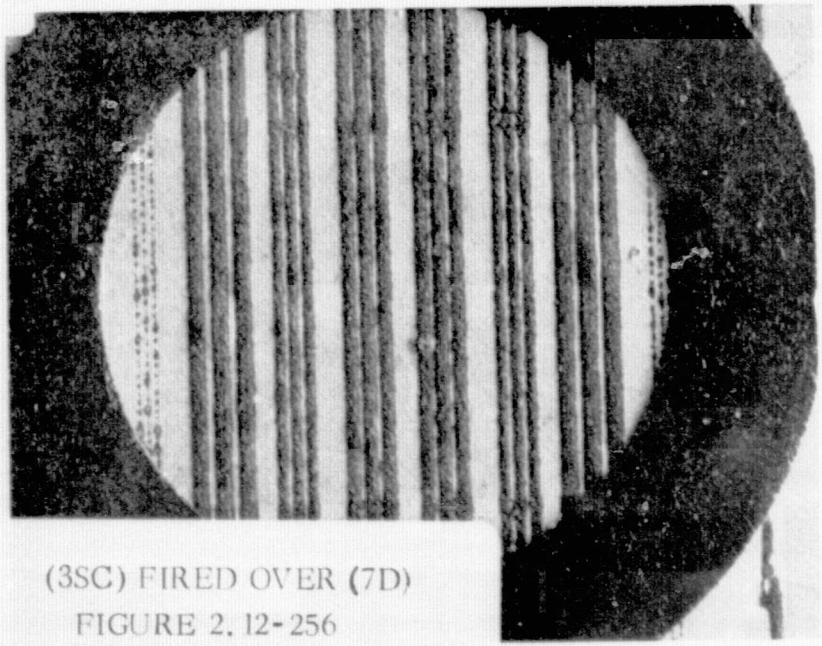
(3SC) FIRED OVER (4D)
FIGURE 2.12-253



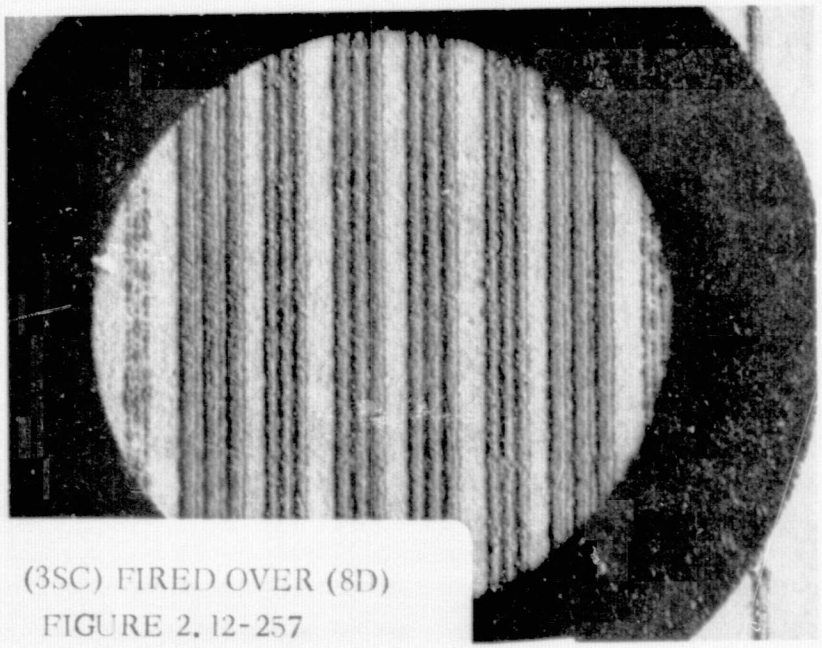
(3SC) FIRED OVER (5D)
FIGURE 2.12-254



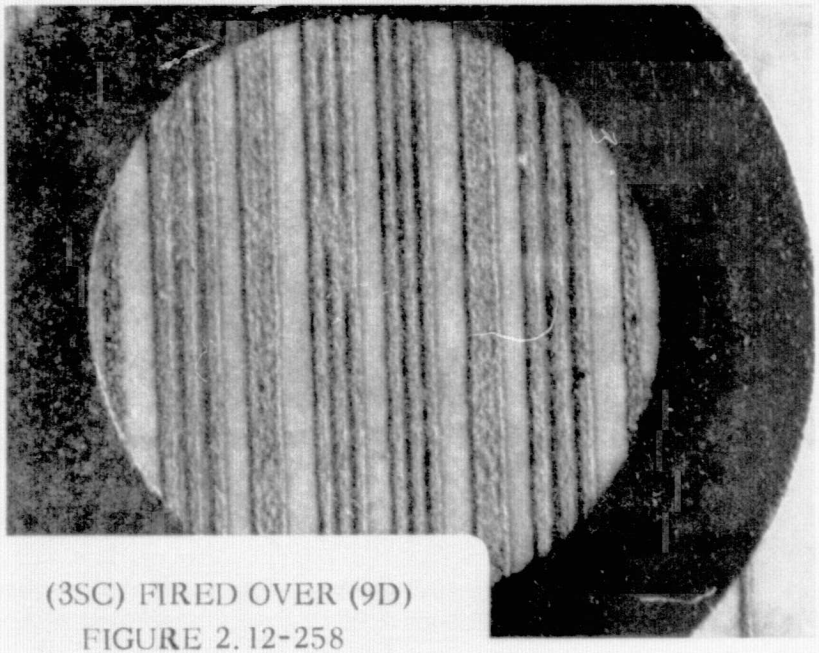
(3SC) FIRED OVER (6D)
FIGURE 2.12-255



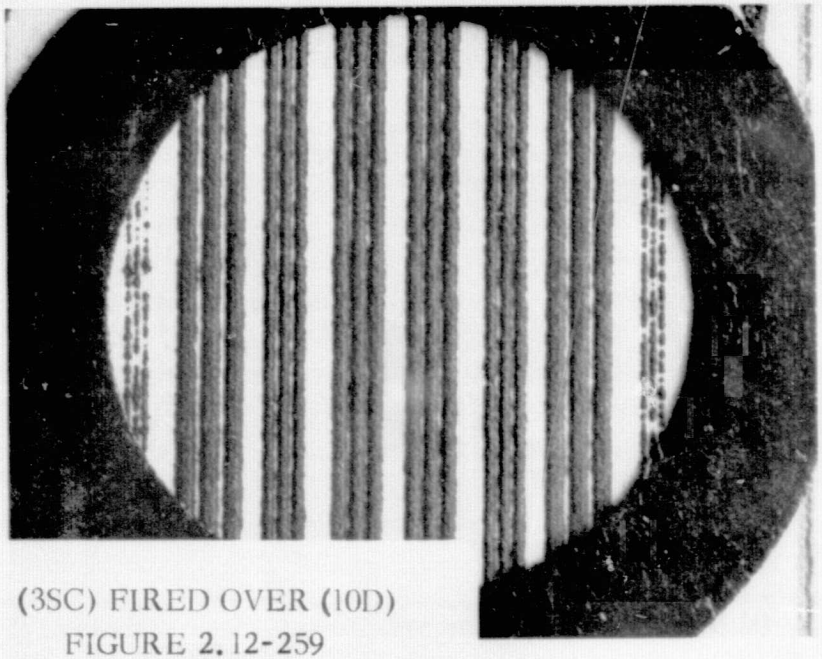
(3SC) FIRED OVER (7D)
FIGURE 2.12-256



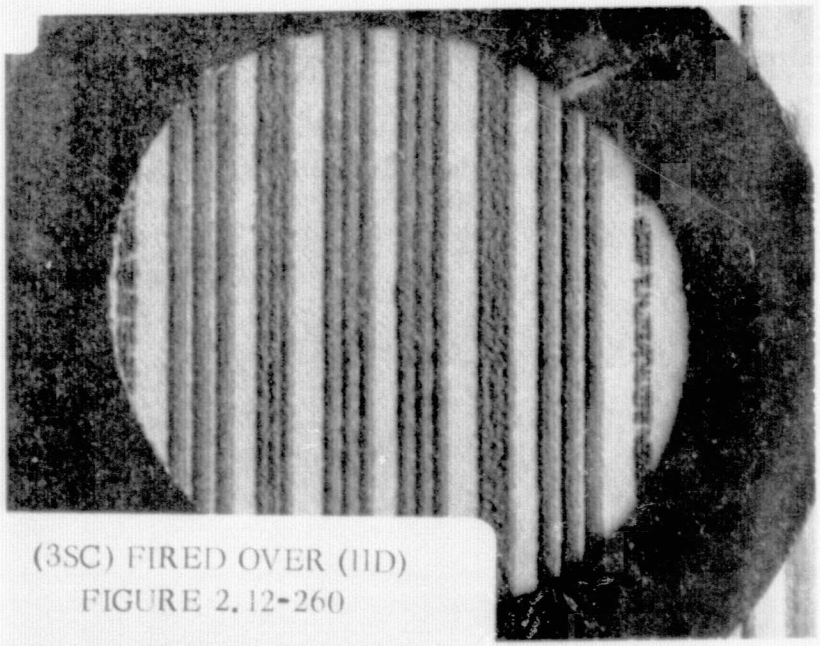
(3SC) FIRED OVER (8D)
FIGURE 2.12-257



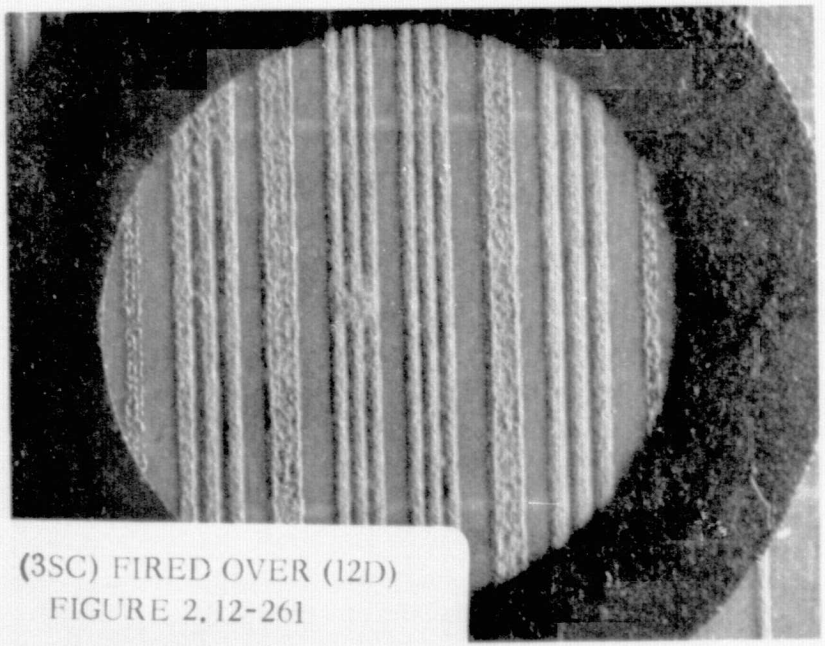
(3SC) FIRED OVER (9D)
FIGURE 2.12-258



(3SC) FIRED OVER (10D)
FIGURE 2.12-259



(3SC) FIRED OVER (11D)
FIGURE 2.12-260



(3SC) FIRED OVER (12D)
FIGURE 2.12-261

It is understood that the combinations shown above may not necessarily be used in multilayer fabrication. It should be noted, also, that combinations of materials may react differently than when processed individually. The reactions and results shown in this evaluation study are the direct results obtained in processing at the ECI Thick Film Laboratory and should be verified or disproved at the discretion of the laboratories intending to use the materials.

Any discussions concerning this evaluation should be directed to the author, Carl J. Peckinpaugh Principal Engineer, Microelectronics Laboratory, Electronic Communications, Inc.

2.13 Conclusions

The observations made during the technical papers study portion of this program were many and varied. It became increasingly obvious as the study progressed that there existed definite similarities in the papers concerned with ceramic multilayer philosophy. The most common similarity was that they all predicted a great and growing future for the technology.

In general, the papers reviewed could be grouped into three different types, the "How To" fabrication type, the "How We Did" recap type, and the "How We Will Do" advance technology type of papers. Most of the papers seemingly applicable to this design guide handbook ("How To" and "How We Will Do") did not possess sufficient individual original information and observations to warrant their data use in a design standard. It appeared in a considerable amount of the papers that an extensive amount of cross referencing was accomplished with little analytical laboratory evaluation to substantiate the observations. It became increasingly apparent that any real meaningful data concerning dimensional limitations would have to be based on a materials capability study using currently available "advanced" materials of fabrication.

The Materials Evaluation Study portion of this program (2.1.2) became a very significant factor in the development of the design guide section. The individual material limitations themselves became the most important factors outside of workmanship standards and equipment utilization in establishing the dimensional limitations and inspection criteria.

The final conclusions drawn from this program must again be based on materials and their limitations. Newer and seemingly better formulations are appearing with increasing regularity. Each new material has its own idiosyncrasies and must be evaluated extensively to determine its capabilities both alone and combined with other materials.

The microelectronics field is as always, a changing field of endeavor with no lasting commitment to any one technology. The tide of interest and application will always turn towards that area which offers the most significant return for the amount of investment. Ceramic multilayer technology does offer considerable opportunity in this regard. The areas of material technology, computer aided design, equipment development, and circuit design application are all developing specialty fields with each reinforcing the other so that ceramic multilayer technology will evolve into a broad based science with a promising future as an electronics packaging methodology.

SECTION 3
GLOSSARY OF TERMS

ALUMINA: Aluminum oxide (Al_2O_3).

AMP: Abbreviation for ampere, unit of current flow. One ampere of current flow is equivalent to one coulomb of charge flowing per second.

AND GATE: A logic gate where all of the inputs must be "1's" before the output is a "1."

ANGLE OF ATTACK: The angle between the squeegee face of a thick film printer and the plane of the screen.

ARRAY: A group of elements or circuits arranged in rows and columns on one substrate.

ASPECT RATIO: The ratio between the length of a film resistor and its width. The number of squares in a thick film resistor ($\frac{L}{W}$).

BACK BONDING: The "conventional" way of bonding active chips to the substrate. The physical attachment is made using the back of the chip, leaving the face, with its circuitry, up. The opposite of back bonding is face bonding – beam leads and flip chips being the most common face bonding approaches.

BALL BONDING: A method of thermocompression bonding where the first bond is made from a "ball" formed when a flame cuts through the wire.

BEAM LEAD: An active chip that can be face bonded where the connections between the chip and the substrate are made by means of

"beams" of plated metal that protrude cantileverlike from the edge of the chip.

BERYLLIA: Beryllium oxide (BeO). A substrate material used where extremely good heat conductivity is desired. Beryllia substrates are excellent electrical insulators but conduct heat better than do most metals.

BLOCK: To plug up an open mesh in a screen.

DIE BONDING Attaching the integrated circuit chip to the substrate.

WIRE BONDING Making electrical interconnections in integrated circuits by attaching fine wire between the IC's face and the substrate's conductor pads.

BRAZING: Similar to soldering, but with hard metals at higher temperatures. Hard soldering.

BREAD-BOARD: The first wiring together of a proposed circuit to evaluate its performance. Originally done by using a wooden board with nails spaced in rows. Individual component leads were wrapped around the nails.

BUMPS: The protuberance on a flip chip through which electrical connection is made to the outside. They also serve to elevate the chip mechanically off the surface of the substrate. They can be on the chip or on the substrate.

C: Abbreviation for capacitance.

CARRIER: A term that describes the amount of overall warpage present in a substrate. Camber is determined by measuring the difference between actual thickness and the separation required of two parallel plates to enable the substrate to fit.

CAPACITOR: A device that can store an electrical charge when voltage is applied. A device whose impedance is inversely proportional to the frequency of the voltage impressed. (That is, it offers little resistance or impedance to high frequencies but much to low frequencies.)

CERAMIC: Inorganic clay-like material molded and formed by high temperature processes.

CONDUCTIVITY: The ability of a material to conduct electricity.

CONDUCTOR: A class of materials that conduct electricity and have a low resistivity (10^{-1} ohm-cm).

CONTACT PRINTING: A method of screen printing where the screen is almost (within a few mils) in contact with the substrate. Used for precision printing or for printing with screens made of nonflexible materials.

CROSSOVER: In a multilayer thick film circuit, a place where two conductors cross. It consists of the two conductors and an insulating material which separates the conductors.

CROSSTALK: Signals from one source interfere with another nearby conductor because of capacitive or inductive coupling.

DIP: Abbreviation for dual-in-line package. Designed primarily for plugging into circuit boards.

DEFINITION: The sharpness of a screen printed pattern - the exactness with which a pattern is printed.

DEGRADATION Change for the worse in the characteristics of an electric element because of heat, high voltage, etc.

DICE: The singular of die. An integrated circuit chip.

DIELECTRICS: Materials that do not conduct electricity. Generally "dielectrics" refers to materials that are to be used as capacitors whereas "insulators" refers to materials that are primarily electrical insulators. The materials can serve as either or both, and the terms have essentially the same meaning.

DIELECTRIC CONSTANT: The terms used to describe a material's ability to store charge when used as a capacitor dielectric. It is the ratio between the charge that would be stored with free space as the dielectric and the material in question. Same as relative permitivity.

DIELECTRIC STRENGTH: The maximum electric field that a dielectric will withstand without breaking down (physically). Expressed in volts per unit distance, such as centimeter, mil, etc.

DIFFUSION: The phenomenon of movement of matter from regions of high concentration to regions of low concentration.

DIRECT EMULSION SCREEN: A screen whose emulsion is applied by painting directly onto the screen – as opposed to the indirect emulsion type.

DISCRETE: As applied to components used in thick film circuits: the elements that are added separately are discrete elements (or devices) as opposed to those that are made by screen printing methods.

DISSIPATION FACTOR: Tengent of the dielectric loss angle. Dissipation factor is the ratio of the resistive component of a capacitor (Rc) to the capacitive reactance (Xc) of the capacitor.

DOCTOR BLADE: A method for casting thin, uniform layers of liquid on a flat surface. Used in making multilayer capacitor chips and alumina substrates.

DOLL: The area needed on a substrate layout for a component and its connections.

DRIFT: Permanent change in value of a capacitor or resistor over a period of time because of the effects of temperature, aging, humidity, etc.

DUAL-IN LINE PACKAGE: See DIP.

DYNAMIC TESTING: Active elements can be tested in two ways: (1) Static, where only DC tests are made, and (2) Dynamic, where reaction to AC (especially high frequency) are evaluated.

E: Symbol for voltage.

EMULSION: The organic material used to coat and/or plug up the mesh of a screen.

ENCAPSULATE: Sealing up or covering an element or circuit for mechanical and environmental protection.

EUTECTIC: The point of the maximum fusibility of a combination of materials. The "eutectic temperature" of a system is always lower than the melting point of any of the individual components of the system.

F: The abbreviation for farad.

FACE BONDING: The opposite of back bonding. A face bonded semiconductor chip is one that has its circuitry side facing the substrate. Flip chip and beam lead bonding are the two common face bonding methods.

FARAD: Unit of capacitance equal to that capacitance that will allow a charge of oue coulomb with a potential of one volt.

FERRO-ELECTRIC: A crystalline dielectric that exhibits dielectric hysteresis – an electrostatic analogy to ferromagnetic materials.

FILTERS: Components or groups of components that can transmit or pass certain frequencies while rejecting others. Low pass filters, high pass filters, band pass filters and band reject filters are the types used.

FIRE: The term used to describe the act of heating a thick film circuit so that the resistors, conductors, capacitors, etc., will be transformed into their final form.

FLAT PACK: One of the popular integrated circuit package configurations. The leads are coplanar with the package and are usually attached to a pc board by welding or soldering rather than by bending and plugging into pc board holes.

FLUX: (1) In soldering, a material that chemically attacks surface oxides and tarnishes so that the molten solder can wet the surfaces to be soldered.

FRIT: Melted glass composition, ground up and used in thick film compositions as the portion of the composition that melts upon firing to give adhesion to the substrate and hold the composition together.

FUSED: Melted.

GREEN: A term used in ceramic technology meaning unfired. For example, a "green" substrate is one that has been formed, but has not been fired. Green and fired in ceramics are synonyous to raw and cooked in foods.

HERMETIC: Sealed up so that it is gas right. The test for hermeticity is to observe leak rates when placed in a vacuum. A plastic encapsulation cannot be hermetic by definition because there is no gas to escape.

HERTZ (Hz): Official terminology in electronics for frequency (replacing the term," cycles").

HI-K: Abbreviation for high dielectric constant.

HOMOGENITY: Alike or uniform in composition. A thick film composition that has settled out is not homogeneous, but after proper stirring it is. The opposite of heterogeneous.

HOT ZONE: The part of a continuous furnace or kiln that is held at maximum temperature. Other zones are the preheat zone and cooling zone.

HYBRID MICRO-CIRCUIT: A microcircuit consisting of elements which are a combination of the film circuit type and the semiconductor types, or a combination of both types with discrete parts.

I: Symbol for current.

IC: Abbreviation for integrated circuit.

IMPEDANCE (Z): The term given to the overall resistance of an assembly of components to the passage of current. Impedance levels (measured in ohms) are often frequency sensitive, being made up of the vector sum of the individual reactances of capacitors (X_C) and inductors (X_L) and of the resistance of resistors (R) in the relationship:

$$Z = \sqrt{R^2 + (X_L + X_C)^2}$$

INDIRECT EMULSION SCREEN: A screen whose emulsion is a separate sheet or film of material, attached by pressing into the mesh of the screen (as opposed to the direct emulsion type).

INDUCTOR: An electronic component that usually consists of a coil of wire. It offers little resistance to low frequencies and much resistance to high frequencies. Not used in integrated circuits as extensively as in conventional circuitry.

$$(X_L = 2 \ \pi \ fL)$$

INK: Synonymous with "composition" and "paste" when relating to screenable thick film materials.

INSULATION RESISTANCE (IR): The resistance of a capacitor to the passage of current when charged, i.e., a measure of its tendency to slowly discharge. IR is measured in megohms.

INSULATORS: A class of materials with high resistivity. Materials that do not conduct electricity. Materials with resistivity values of over 10^5 ohm-cm are generally classified as insulators.

INTEGRATED CIRCUIT: A microcircuit consisting of interconnected elements inseparably associated and formed in situ on or within a single substrate to perform an electronic circuit function.

INTERFACE: The borderline region between two different thick film materials as the region where a thick film resistor composition and its connecting conductor composition meet and intermingle, react, etc.

K: Symbol for dielectric constant.

KOVAR": Westinghouse Electric Company's trademark for metal alloy consisting of nickel, iron, and cobalt. Its thermal expansion is low, closely matching that of glass and ceramic materials.

L: Symbol for inductance.

LEACHING: In soldering, the dissolving (alloying) of the material to be soldered into the molten solder.

LEVELING: A term describing the settling or smoothing out that takes place after a pattern is screen printed. Immediately after printing, the mesh marks of the screen are visible. With compositions that have good leveling, characteristics, these marks disappear quite rapidly (healing).

LID: Abbreviation for "leadless Inverted Device." A packaging scheme for integrated circuits and transistors especially adapted for use with hybrid circuits.

LINE DEFINITION: A descrptive term indicating a capability of producing sharp, clean, screen printed lines. Capability is often described in terms of the line width and spacing that is possible – such as 3 X 3, indicating line definition capabilities of 3 mil lines and 3 mil spaces.

LOGIC GATE: A circuit that is a basic building block of computers. Different types, such as AND, OR, and different capacities, such as 3, 4, or more inputs, describes a gate.

LSI: Large scale integration. An integration circuit with an equivalent of 100 or more gates in a single chip.

MASK: The photographic negative that serves as the master for making thick filn screens.

MESH SIZE: The number of openings per inch in a screen. A 200 mesh screen has 200 openings per linear inch, 40, 000 openings per square inch.

METAL MASK (SCREENS): A screen made not from wire or nylon thread but from a solid sheet of metal in which holes have been etched in the desired pattern. Useful for precision and/or fine printing.

METRIC PREFIXES: Prefixes that indicate a fraction or a multiple of the main term, as picofarad, microampere,

giga = 10^{9}	milli = 10^{-3}
mega = 10^{6}	micro = 10^{-6}
kilo = 10^{3}	pico = 10^{-12}

mfd: Abbreviation for microfarad (10^{-6} farad).

MICRO-CIRCUIT: A small circuit having a high equivalent circuit elment density, which is considered as a single part composed of interconnected elements on or within a single substrate to perform an electronic circuit function.

MICRO-ELECTRONICS: That area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

MICROWAVE: Short wave transmissions. Frequencies above several hundred megahertz are considered microwave. A gigahertz has a wavelength of 30 centimeters.

MIL: One thousandth of an inch, 10^{-3} inches, equivalent to 25 microns.

MISMATCH: THERMAL: The difference between the thermal expansion of two materials.

MOLY-MANGANESE: The base materials used in many ceramic packages where gold plating or glass sealing is planned. The molybdenum manganese material is supplied to alumina and then fired in reducing atmospheres at temperatures above 2500^{o}F. It produces high adhesion and will take plating readily.

MONOLITHIC: A term sometimes used to indicate a multilayer ceramic chip capacitor.

MONOLITHIC INTEGRATED CIRCUIT: An integrated circuit consisting of elements formed on or within a semiconductor substrate with at least one of the elements formed within the substrate.

MULTICHIP MICRO-CIRCUIT: A microcircuit consisting of elements formed on or within two or more semiconductor chips which are separately attached to a substrate.

MULTILAYER CERAMIC CAPACITOR: A miniature ceramic capacitor manufactured by paralleling several thin layers of ceramic.

MULTILAYER CIRCUITS: Circuits with more than one plane or level of conductors. The complexity of some circuits is more than can be handled with one level of conductors because of need for high density and many crossovers.

MULTILAYER SUBSTRATES: Substrates that have buried conductors so that complex circuitry can be handled.

NAND GATE: A logic gate whose output is the reverse of an AND gate. (If all inputs are "1" the output is "0.")

NOISE: Random small variations in voltage or current in a circuit due to the quantum nature of electronic current flow, thermal considerations, etc.

NOR GATE: A logic gate whose output is the opposite of an OR gate. (If any input is a "1', the output will be "0.")

NPO: EIA code for capacitor temperature characteristic, meaning "Negative-Positive-Zero." A capacitor with no change in capacitance with temperature.

OFF CONTACT: The opposite of contact printing in that the printer is set up with a space between the screen and the substrate.

OHM: The unit of resistance (R) or impedance (Z). Ohm's law states that Z = E/I. In the case of resistance only, R = E/I. A voltage of 1 volt produces a 1 amp current if the material has a 1 ohm resistance.

OHM/SQUARE: The unit of sheet resistance, or more properly, of sheet resistivity.

OR GATE: A logic gate which will put out a "1" if any of the inputs are a "1."

OVERGLAZE: A glass coating that is over another component or element, normally for physical or electrical protection purposes.

PACKAGE: In integrated circuits, the arrangement for protecting the circuit from the outside world, furnishing leads in the proper configuration, etc.

PAD: The metallized area on a substrate or on the face of an integrated circuit used for making electrical connections.

PARTITIONING: The part of the job of designing an electronic system concerned with dividing it into individual circuits.

PASSIVE COMPONENTS (ELEMENTS): Elements (or components) that have no capabilities of amplification. Capacitors, inductors and resistors are passive components. Transistors and electron tubes are active components.

PASTE: Synonymous with "composition" and "ink" when relating to screenable thick film materials.

PEEL STRENGTH: A measure of adhesion between a conductor and the substrate. The test is performed by pulling or peeling the conductor off the substrate and observing the force required. Units are oz/mil or lb/in of conductor width.

pf: Abbreviation for picofarad (10^{-12} farad).

PF: Abbreviation for power factor.

PHASE: Refers to the part or portion of a materials system that is metallic or glossy in nature.

PINHOLE: In thin dielectrics, such as screen printed capacitors, a bubble results in a small void (extending sometimes across the entire thickness of the dielectric). This is called a pinhole.

POLY-CRYSTALLINE: A material is polycrystalline in nature if it is made of many small crystals. Alumina ceramics are polycrystalline, whereas glass substrates are not.

PREFORM: To aid in soldering, small circles or squares of the solder are punched out of thin sheets. These preforms are placed on the spot to be soldered or bonded, prior to placing the object to be attached, such as silicon chip.

"PRINT AND FIRE" A term sometimes used to indicate the thick film process.

PROFILE: A graph of time versus temperature, or of position in a continuous thick film furance versus temperature.

PURPLE PLAGUE: A gold aluminum compound sometimes formed when bonding gold to aluminum as with wire bonding silicon chips. Purple

plague is purplish in color and is very brittle, thus making a dangerously unreliable bond.

Q: Quality factor. The repicrocal of dissipation factor. The higher the number, the less the losses of a capacitor. Used mostly where dissipation factor is low, below. 001 (Q = 1000).

REFLOW SOLDERING: A method of soldering involving application of solder to the parts to be soldered prior to the actual joining. To solder, the parts are joined and heated, causing the solder to remelt, or reflow.

RESIST: A protective coating that will keep another material from attaching itself or coating something – as in solder resist or plating resist.

RESISTANCE: The term used to indicate relative "resistance" to current flow of an object when voltage is applied. Ohm's law states: R = E/I. The unit of resistance is "ohm."

RESISTIVITY: The material characteristic that has to do with resistance to electrical current flow. The relationship between resistance (R) and resistivity (ρ) is: $R = L/\rho \quad A$.

RESISTOR: A device that offers resistance to the flow of electrical current in accordance with Ohm' s law: R = E/I.

RESOLUTION: The degree of fineness or detail of a screen printed pattern.

RF: Abbreviation for radio frequency.

RHEOLOGY: The science dealing with deformation and flow of matter.

RISERS: The conductive paths that run vertically from one level of conductors to another in a multilayer substrate or screen printed thick film circuit.

RUBYLITH: Ulano Company's trademark for a popular masking film. It consists of a transparent MYLAR sheet with a strippable red film coating. Used in preparing integrated circuit artwork.

SCREEN: Term for the screen used in thick film printing.

SCRUB: In die bonding, the movement of the chip (ultrasomic or mechical) under pressure on the bonding pad surface to make an improved metallurgical contact.

SEMI-CONDUCTORS: A class of materials with resistivity values between those of conductors and insulators.

SHEET RESISTIVITY: The resistance of a film of material with the same length and width, i.e., one "square." The resistivity of thick film resistor compositions is expressed in terms of sheet resistivity (ohms/square).

SLUMP: A spreading of printed thick film composition after screen printing but before drying. Too much slumping results in loss of definition.

SLURRY: A thick mixture of liquid and solids, the solds being in suspension in the liquid.

SNAP-OFF DISTANCE: The screen printer distance setting between the bottom of the screen and top of the substrate.

SQUEEGEE: The part of a screen printer that pushes the composition across the screen and through the mesh onto the substrate.

STANDARD DEVIATION: A statistical term that helps describe the likely value of parts in a lot or batch of components in comparison with the lot's average value. Practically all of a lot will fall within ±3 standard deviations of the average value.

STATIC TESTING: Testing of IC chip with DC only – the opposite of dynamic testing.

STEATITE: A ceramic consisting primarily of magnesium silicate popularly used as an electrical insulator. Rarely used as a thick film substrate.

STITCH BONDING: One of the methods of wire bonding. Consists of pressing the wire onto the conductor pad. Bonding is achieved by ultrasonic or thermocompression energy.

SUBSTRATE: The supporting material upon or within which the elements of a microcircuit or integrated circuit are fabricated or attached.

SWIMMING: Lateral shifting of a thick film conductor pattern on molten glass crossover patterns.

TC: Abbreviation for thermocompression (bonding); also abbreviation for temperature coefficient (resistors and capacitors).

TCR: Temperature coefficient of resistance.

TEMPERATURE COEFFICIENT OF RESISTANCE: The amount of resistance change of a resistor (or resistor material) with temperature – commonly expressed as average change over a certain temperature range in parts per million per degree Centigrade (ppm/^{o}C).

THERMO-COMPRES-SION BONDING: A method of wire bonding integrated circuits where temperature and pressure are the methods of obtaining the bond between wire and pad.

THICK FILM: A film deposited by screen printing processes and fired at high temperatures to mature into its final form. The basic process of thick film integrated circuits is the screen printing and firing process.

THIXO-TROPIC: A fluid that gets less viscous as it is stirred (or moved) faster is thixotropic. Most thick film compositions are thixotropic. A material that has a nonlinear stress shear ratio which decreases with increasing stress is thixotropic.

TINNED: Literally, coated with tin, but commonly used to indicate coated with solder.

TO: A series of metal packages originally designed for transistors, but used extensively for integrated circuits.

TRACKING: Two resistors on the same circuit that change resistance with temperature in close harmony are said to track well. Tracking of different resistors is measured in ppm/^{o}C (difference). Tracking is also used in reference to temperature hysteresis performance and potentiometer repeatibility.

TRIM: To change value from "as fired" to the final desired value, usually by removing parts of the body of the resistor.

ULTRA-SONIC: A method of cleaning that uses cavitation in fluids caused by applying ultrasonic vibrations to the fluid. A method of bonding wire to integrated circuits that uses ultrasonic energy to effect

the metallurgical bond between the metal of the wire and of the pads.

VCR: Abbreviation for voltage coefficient of resistance.

VEHICLE: A thick film term that refers to the organic system in the composition.

VIAS: Same as risers.

VISCOSITY: A term used to describe the fluidity of material, or the rate of flow versus pressure. The unit of viscosity measurement is poise – more commonly centipoise.

VITREOUS: Glassy. A term used in ceramic technology indicating fired characteristics approaching being glassy, but not necessarily totally glassy.

VOLT: Unit of electrical potential. The potential between two points which requires 1 joule of work to bring a 1 coulomb charge from one point to the other.

VOLUME RESISTIVITY: A 1-cm cube of material will have resistance equal to the material's resistivity. The qualification volume adds nothing, but is sometimes used so that "resistivity" and "resistance" will not be confused.

W5R: E1A capacitor code, meaning less than 15% capacitance change between $-55^{\circ}C$ and $+125^{\circ}C$.

ZENER: A special kind of diode that allows no current flow until a certain voltage is reached.

SECTION 4

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